Artix FPGA On Module (FOM)

REV	Description	DATE	BY
0	PRELIMINARY prototype release for review. Not manufactured yet.	01/10/2018	ws
0.1	Added wireless socket to the Abone. Not manufactured yet.	01/16/2018	ws
0.9	Changed DDR3 to ZBT. Reassigned Hirose pins. Not manufactured yet.	07/14/2018	ws

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
A - Revision page

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 1 of 29

Artix configuration pins

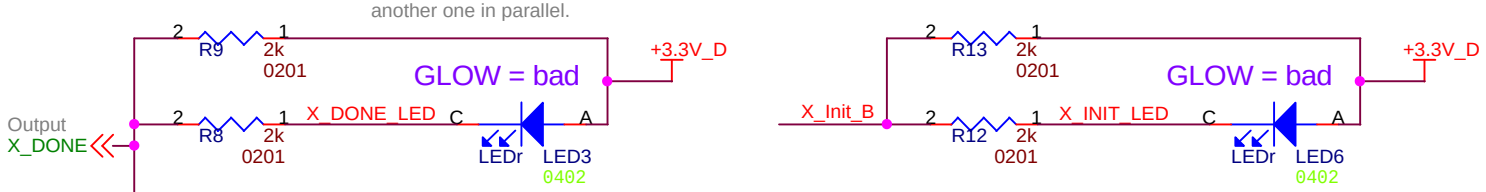
XC7A15T-1CSG324C $32
XC7A15T-2CSG324C $37
XC7A15T-3CSG324E $49

XC7A35T-1CSG324C $43
XC7A35T-2CSG324C $49
XC7A35T-3CSG324E $65

XC7A100T-1CSG324C $126
XC7A100T-2CSG324C $134
XC7A100T-3CSG324E $177

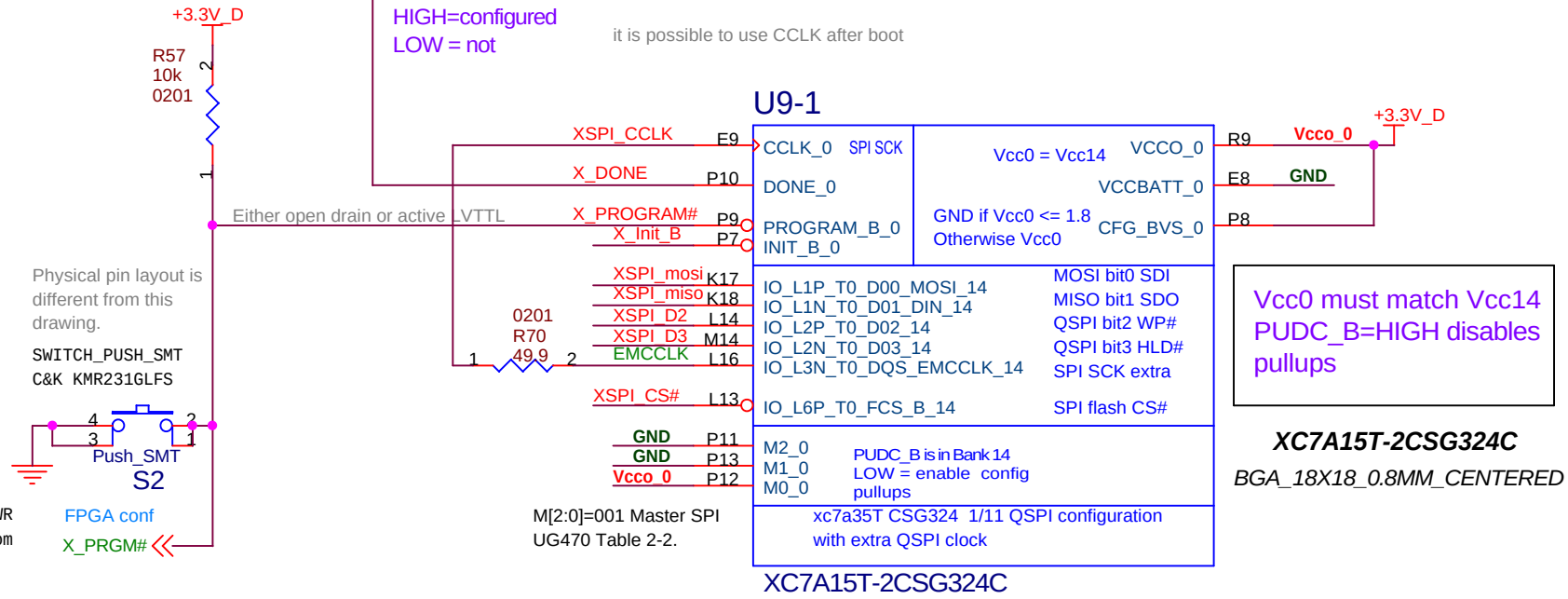
APHHS1005CGCK	grn	40 mcd
APHHS1005SYCK	yllw	150 mcd
APHHS1005SECK	orng	150 mcd
APHHS1005SURCK	red	70 mcd
APHHS1005QBC/D	blue	60 mcd

LED is not a good pullup, so we need another one in parallel.



HIGH=configured
LOW = not

it is possible to use CCLK after boot



Vcc0 must match Vcc14
PUDC_B=HIGH disables pullups

XC7A15T-2CSG324C

BGA_18X18_0.8MM_CENTERED

Physical pin layout is different from this drawing.

SWITCH_PUSH_SMT
C&K KMR231GLFS

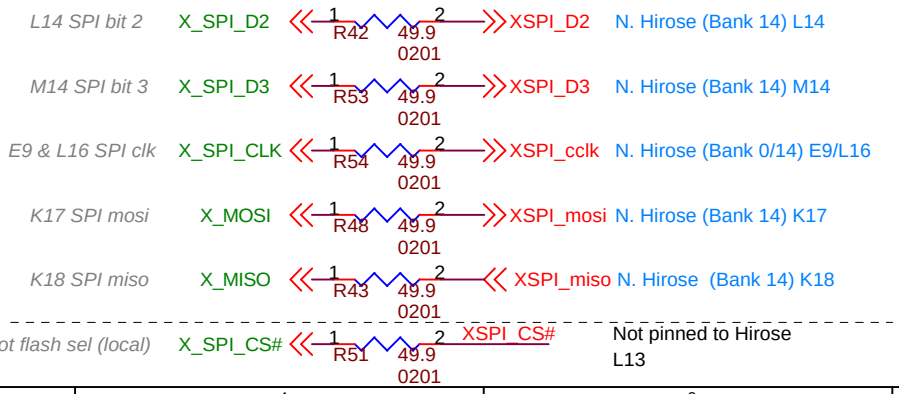
RESET from PWR module or from motherboard

FPGA conf
X_PRGM#

M[2:0]=001 Master SPI
UG470 Table 2-2.

Wires adjacent to the flash chips

Wires between the FPGA and N.Hirose



GND

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents: Artix configuration pins

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 2 of 29

Artix Bank 14

Must be the same as Bank 0.
Use the same Vcc as flash.

This bank contains some configuration pins.

SGMII can be implemented in 3.3V bank. LVDS reception works at any Vcco with external termination. (Internal termination requires 2.5V.). LVDS transmission requires 2.5V, but TMDS can be used at Vcco=3.3V.

Banks 0 and 14 are the only ones with guaranteed 3.3V. Other banks may be setup for any Vcco. Consequently, the main clock has to be connected here.

+3.3V_D +Vcco_bank14

LVDS out requires using 2.5V.
LVDS in and TMDS permit 3.3V

U9-2

50 I/O per bank

IO_0_14
IO_25_14

K18: IO_L1N_T0_D01_DIN_14
K17: IO_L1P_T0_D00_MOSI_14
M14: IO_L2N_T0_D03_14
L14: IO_L2P_T0_D02_14
L16: IO_L3N_T0_DQS_EMCCLK_14

config IO_L3P_T0_DQS_PUDC_B_14
IO_L4N_T0_D05_14
IO_L4P_T0_D04_14
IO_L5N_T0_D07_14
IO_L5P_T0_D06_14
IO_L6N_T0_D08_VREF_14
L13: IO_L6P_T0_FCS_B_14
IO_L7N_T1_D10_14
IO_L7P_T1_D09_14
IO_L8N_T1_D12_14
IO_L8P_T1_D11_14
IO_L9N_T1_DQS_D13_14
IO_L9P_T1_DQS_14
IO_L10N_T1_D15_14
IO_L10P_T1_D14_14
IO_L11N_T1_SRCC_14
IO_L11P_T1_SRCC_14
IO_L12N_T1_MRCC_14
IO_L12P_T1_MRCC_14
IO_L13N_T2_MRCC_14
IO_L13P_T2_MRCC_14
IO_L14N_T2_SRCC_14
IO_L14P_T2_SRCC_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L16N_T2_A15_D31_14
IO_L16P_T2_CSI_B_14
IO_L17N_T2_A13_D29_14
IO_L17P_T2_A14_D30_14
IO_L18N_T2_A11_D27_14
IO_L18P_T2_A12_D28_14
IO_L19N_T3_A09_D25_VREF_14
IO_L19P_T3_A10_D26_14
IO_L20N_T3_A07_D23_14
IO_L20P_T3_A08_D24_14
IO_L21N_T3_DQS_A06_D22_14
IO_L21P_T3_DQS_14
IO_L22N_T3_A04_D20_14
IO_L22P_T3_A05_D21_14
IO_L23N_T3_A02_D18_14
IO_L23P_T3_A03_D19_14
IO_L24N_T3_A00_D16_14
IO_L24P_T3_A01_D17_14

xc7a35T CSG324 2/11

XC7A15T-2CSG324C

+Vcco_bank14
L17 VCCO_14
N13 VCCO_14
P16 VCCO_14
T12 VCCO_14
U15 VCCO_14
V18 VCCO_14
Vcco14 = Vcc0

R11 IO_14_0_r11 Single ended R11
R10 IO_14_25_r10 Single ended R10

1 10k R84 0201 2 GND PUDC_B=LOW enables pullups

L15 IO_14_L3P_PUDC_L15 L15 PUDC S.Hirose
M18 IO_14_L4N_m18 M18 S.Hirose
L18 IO_14_L4P_L18 L18 S.Hirose
R13 IO_14_L5N_r13 R13
R12 IO_14_L5P_r12 R12
M13 IO_14_L6N_m13 M13 S.Hirose
L6P = boot flash
T18 SGMII_MDIO_CLK T18 - up to 25MHz
R18 SGMII_MDIO_DATA R18 - up to 25MHz
P14 IO_14_L8N_p14 P14
N14 IO_14_L8P_n14 N14
P18 IO_14_L9N_p18 P18 S.Hirose
N17 IO_14_L9P_n17 N17 S.Hirose
M17 IO_14_L10N_m17 M17 S.Hirose
M16 IO_14_L10P_m16 M16 S.Hirose
N16 IO_14_L11N_n16 N16 S.Hirose
N15 IO_14_L11P_n15 N15 S.Hirose
R17 IO_14_L12N_r17 R17 S.Hirose sngl
P17
R15 IO_14_L13N_r15 R15 S.Hirose
P15 SGMII_Synch_CLK p15 125MHz from PHY (synch Ether)
T15 IO_14_L14N_t15 Bank_14_SRCC_T15
T14 IO_14_L14P_t14 Bank_14_SRCC_T14
T16 IO_14_L15N_t16 T16
R16 IO_14_L15P_r16 R16
V16 SGMII_interrupt V16
V15 X_SPI_SSD_CS# v15 SSD CS# "disk"
U18 SGMII_to_PHY- u18 TMDS_33 to PHY
U17 SGMII_to_PHY+ u17 TMDS_33 to PHY
V17 SGMII_from_PHY- v17 LVDS_25 to FPGA
U16 SGMII_from_PHY+ u16 LVDS_25 to FPGA
U11 IO_14_L19N_u11 Bank_14_U11
T11 IO_14_L19P_t11 Bank_14_T11
V12 IO_14_L20N_v12 Bank_14_V12
U12 IO_14_L20P_u12 Bank_14_U12
V11 IO_14_L21N_v11 Bank_14_V11
V10 IO_14_L21P_v10 Bank_14_V10
V14 IO_14_L22N_v14 Bank_14_V14
U14 IO_14_L22P_u14 Bank_14_U14
U13 IO_14_L23N_u13 Bank_14_U13
T13 IO_14_L23P_t13 Bank_14_T13
T10 IO_14_L24N_t10 Bank_14_T10
T9 IO_14_L24P_t9 Bank_14_T9

I2C bus

I2C data
I2C_DATA
1 4.99k R87 0201 2 +3.3V_D
2 49.9 R86 0201 1 R15 S.Hirose IO_14_L13N_r15

I2C_CLK
I2C clock
1 4.99k R88 0201 2 +3.3V_D
2 49.9 R85 0201 1 IO_14_L6N_m13 M13 S.Hirose

System clock

CLK_25MHz_1V8
To Ethernet PHY
GND 1 49.9 R61 2
Voltage swing
3.3/2=1.65V
1 49.9 R60 2 CLK_25MHz
CLK_25MHz_3V3 1 R59 49.9 0201 2

+3.3V_D
20 mA
Y1
4 V+ ENA 1
3 OUT GND 2
25MHz
+3.3V_D
C45 0.1uF 0201

KC3225A25.0000C30E00 50ppm
KC3225A25.0000C3GE00 50ppm
25 MHz
3.2mm x 2.5mm

SGMII termination

2 49.9 R63 1 SGMII_from_PHY- LVDS
2 49.9 R65 1 SGMII_from_PHY+

+3.3V_D
2 49.9 R66 1 SGMII_to_PHY- TMDS
2 49.9 R68 1 SGMII_to_PHY+

FPGA from PHY: LVDS_25 in
FPGA to PHY: TMDS_33 out

100 MHz not used

KC3225A100.000C3GE00 50ppm
KC3225A100.000C30E00 50ppm
ETXO-H33CL-100.000 2.5ppm
100 MHz
3.2mm x 2.5mm

XC7A15T-2CSG324C
BGA_18X18_0.8MM_CENTERED

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

GND

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
Artix bank 14

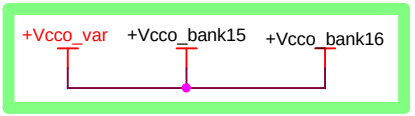
Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 3 of 29

Artix Banks 15 and 16
Variable Vcco

This bank does not contain configuration pins.

LVDS out requires using 2.5V. LVDS in and TMDS permit 3.3V



+Vcco_bank15

U9-3

A17	VCCO_15	Vcc0 = Vcc15	IO_0_15	G13	IO_15_0_g13 G13 (Bank 15, SE)
C13	VCCO_15		IO_25_15	K16	IO_15_25_k16 K16 (Bank 15, SE)
D16	VCCO_15		IO_L1N_T0_AD0N_15	C14	IO_15_L1N_c14 C14 (Bank 15)
G15	VCCO_15		IO_L1P_T0_AD0P_15	D14	IO_15_L1P_d14 D14 (Bank 15)
H18	VCCO_15		IO_L2N_T0_AD8N_15	B14	IO_15_L2N_b14 B14 (Bank 15)
K14	VCCO_15		IO_L2P_T0_AD8P_15	B13	IO_15_L2P_b13 B13 (Bank 15)
			IO_L3N_T0_DQS_AD1N_15	B12	IO_15_L3N_b12 B12 (Bank 15)
			IO_L3P_T0_DQS_AD1P_15	C12	IO_15_L3P_c12 C12 (Bank 15)
			IO_L4N_T0_15	A11	IO_15_L4N_a11 A11 (Bank 15)
			IO_L4P_T0_15	B11	IO_15_L4P_b11 B11 (Bank 15)
			IO_L5N_T0_AD9N_15	F14	IO_15_L5N_f14 F14 (Bank 15)
			IO_L5P_T0_AD9P_15	F13	IO_15_L5P_f13 F13 (Bank 15)
			IO_L6N_T0_VREF_15	D13	IO_15_L6N_d13 D13 (Bank 15)
			IO_L6P_T0_15	D12	IO_15_L6P_d12 D12 (Bank 15)
			IO_L7N_T1_AD2N_15	B17	IO_15_L7N_b17 B17 (Bank 15)
			IO_L7P_T1_AD2P_15	B16	IO_15_L7P_b16 B16 (Bank 15)
			IO_L8N_T1_AD10N_15	A16	IO_15_L8N_a16 A16 (Bank 15)
			IO_L8P_T1_AD10P_15	A15	IO_15_L8P_a15 A15 (Bank 15)
			IO_L9N_T1_DQS_AD3N_15	A14	IO_15_L9N_a14 A14 (Bank 15)
			IO_L9P_T1_DQS_AD3P_15	A13	IO_15_L9P_a13 A13 (Bank 15)
			IO_L10N_T1_AD11N_15	A18	IO_15_L10N_a18 A18 (Bank 15)
			IO_L10P_T1_AD11P_15	B18	IO_15_L10P_b18 B18 (Bank 15)
			IO_L11N_T1_SRCC_15	E16	IO_15_L11N_e16 E16 (Bank 15) srcc
			IO_L11P_T1_SRCC_15	E15	IO_15_L11P_e15 E15 (Bank 15) srcc
			IO_L12N_T1_MRCC_15	C15	IO_15_L12N_c15 C15 (Bank 15) mrcc
			IO_L12P_T1_MRCC_15	D15	IO_15_L12P_d15 D15 (Bank 15) mrcc
			IO_L13N_T2_MRCC_15	G16	IO_15_L13N_g16 G16 (Bank 15) mrcc
			IO_L13P_T2_MRCC_15	H16	IO_15_L13P_h16 H16 (Bank 15) mrcc
			IO_L14N_T2_SRCC_15	F16	IO_15_L14N_f16 F16 (Bank 15) srcc
			IO_L14P_T2_SRCC_15	F15	IO_15_L14P_f15 F15 (Bank 15) srcc
			IO_L15N_T2_DQS_ADV_B_15	G14	IO_15_L15N_g14 G14 (Bank 15)
			IO_L15P_T2_DQS_15	H14	IO_15_L15P_h14 H14 (Bank 15)
			IO_L16N_T2_A27_15	D17	IO_15_L16N_d17 D17 (Bank 15)
			IO_L16P_T2_A28_15	E17	IO_15_L16P_e17 E17 (Bank 15)
			IO_L17N_T2_A25_15	J13	IO_15_L17N_j13 J13 (Bank 15)
			IO_L17P_T2_A26_15	K13	IO_15_L17P_k13 K13 (Bank 15)
			IO_L18N_T2_A23_15	G17	IO_15_L18N_g17 G17 (Bank 15)
			IO_L18P_T2_A24_15	H17	IO_15_L18P_h17 H17 (Bank 15)
			IO_L19N_T3_A21_VREF_15	H15	IO_15_L19N_h15 H15 (Bank 15)
			IO_L19P_T3_A22_15	J14	IO_15_L19P_j14 J14 (Bank 15)
			IO_L20N_T3_A19_15	C17	IO_15_L20N_c17 C17 (Bank 15)
			IO_L20P_T3_A20_15	C16	IO_15_L20P_c16 C16 (Bank 15)
			IO_L21N_T3_DQS_A18_15	D18	IO_15_L21N_d18 D18 (Bank 15)
			IO_L21P_T3_DQS_15	E18	IO_15_L21P_e18 E18 (Bank 15)
			IO_L22N_T3_A16_15	F18	IO_15_L22N_f18 F18 (Bank 15)
			IO_L22P_T3_A17_15	G18	IO_15_L22P_g18 G18 (Bank 15)
			IO_L23N_T3_FWE_B_15	J18	IO_15_L23N_j18 J18 (Bank 15)
			IO_L23P_T3_FOE_B_15	J17	IO_15_L23P_j17 J17 (Bank 15)
			IO_L24N_T3_RS0_15	J15	IO_15_L24N_j15 J15 (Bank 15)
			IO_L24P_T3_RS1_15	K15	IO_15_L24P_k15 K15 (Bank 15)

xc7a35T CSG324 3/11

XC7A15T-2CSG324C

+Vcco_bank16

U9-4

B10	VCCO_16	IO_L6N_T0_VREF_16	D9	IO_16_L6N_d9 D9 (Bank 16) N.Hirose
		IO_L11N_T1_SRCC_16	B9	IO_16_L11N_b9 B9 (Bank 16) srcc S.Hirose
		IO_L11P_T1_SRCC_16	C9	IO_16_L11P_c9 C9 (Bank 16) srcc S.Hirose
		IO_L12N_T1_MRCC_16	A8	IO_16_L12N_a8 A8 (Bank 16) mrcc- S.Hirose
		IO_L12P_T1_MRCC_16	B8	IO_16_L12P_b8 B8 (Bank 16) mrcc+ S.Hirose
		IO_L13N_T2_MRCC_16	C10	IO_16_L13N_c10 C10 (Bank 16) mrcc S.Hirose
		IO_L13P_T2_MRCC_16	C11	IO_16_L13P_c11 C11 (Bank 16) mrcc S.Hirose
		IO_L14N_T2_SRCC_16	A9	IO_16_L14N_a9 A9 (Bank 16) srcc S.Hirose
		IO_L14P_T2_SRCC_16	A10	IO_16_L14P_a10 A10 (Bank 16) srcc S.Hirose
		IO_L19N_T3_VREF_16	D10	IO_16_L19N_d10 D10 (Bank 16) N.Hirose

xc7a35T CSG324 4/11

XC7A15T-2CSG324C

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

XC7A15T-2CSG324C

BGA_18X18_0.8MM_CENTERED

GND

SkuTek Instrumentation

150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents: Artix banks 15, 16

Size	Document Number	Rev
Custom	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 4 of 29

Artix ZBT Bank 35 and Bank 34 with the rest of ZBT

50 I/O per bank

Vdd = 2.5V or 3.3V

LVDS out requires 2.5V. LVDS in can be used at either 2.5 or 3.3V.
However, diff termination requires 2.5V.

+Vdd_ZBT

U9-6

A7	VCCO_35	IO_0_35	F5 ZBT_data9
C3	VCCO_35	IO_25_35	J5 ZBT_data2
D6	VCCO_35	IO_L1N_T0_AD4N_35	C5 ZBT_A4
F2	VCCO_35	IO_L1P_T0_AD4P_35	C6 ZBT_data27
G5	VCCO_35	IO_L2N_T0_AD12N_35	B6 ZBT_A9
J1	VCCO_35	IO_L2P_T0_AD12P_35	B7 ZBT_A18
		IO_L3N_T0_DQS_AD5N_35	A5 ZBT_A6
		IO_L3P_T0_DQS_AD5P_35	A6 ZBT_A13
		IO_L4N_T0_35	C7 ZBT_data31
		IO_L4P_T0_35	D8 ZBT_data28
		IO_L5N_T0_AD13N_35	E5 ZBT_data22
		IO_L5P_T0_AD13P_35	E6 ZBT_data26
		IO_L6N_T0_VREF_35	D7 ZBT_data25
		IO_L6P_T0_35	E7 ZBT_data24
		IO_L7N_T1_AD6N_35	B4 ZBT_A17
		IO_L7P_T1_AD6P_35	C4 ZBT_clk
		IO_L8N_T1_AD14N_35	A3 ZBT_A12
		IO_L8P_T1_AD14P_35	A4 ZBT_A5
		IO_L9N_T1_DQS_AD7N_35	A1 ZBT_A0
		IO_L9P_T1_DQS_AD7P_35	B1 ZBT_A7
		IO_L10N_T1_AD15N_35	B2 ZBT_A1
		IO_L10P_T1_AD15P_35	B3 ZBT_A8
		IO_L11N_T1_SRCC_35	D4 ZBT_data16
		IO_L11P_T1_SRCC_35	D5 ZBT_A16
		IO_L12N_T1_MRCC_35	D3 ZBT_data18
		IO_L12P_T1_MRCC_35	E3 ZBT_data17
		IO_L13N_T2_MRCC_35	F3 ZBT_data13
		IO_L13P_T2_MRCC_35	F4 ZBT_data21
		IO_L14N_T2_SRCC_35	D2 ZBT_data20
		IO_L14P_T2_SRCC_35	E2 ZBT_data15
		IO_L15N_T2_DQS_35	G2 ZBT_adv_LD#
		IO_L15P_T2_DQS_35	H2 ZBT_data11
		IO_L16N_T2_35	C1 ZBT_ben_2
		IO_L16P_T2_35	C2 ZBT_ben_3
		IO_L17N_T2_35	G1 ZBT_RW#
		IO_L17P_T2_35	H1 ZBT_A10
		IO_L18N_T2_35	E1 ZBT_data12
		IO_L18P_T2_35	F1 ZBT_data8
		IO_L19N_T3_VREF_35	F6 ZBT_data30
		IO_L19P_T3_35	G6 ZBT_data29
		IO_L20N_T3_35	G3 ZBT_data10
		IO_L20P_T3_35	G4 ZBT_data14
		IO_L21N_T3_DQS_35	H4 ZBT_data0
		IO_L21P_T3_DQS_35	J4 ZBT_data1
		IO_L22N_T3_35	J2 ZBT_A11
		IO_L22P_T3_35	J3 ZBT_data4
		IO_L23N_T3_35	K1 ZBT_A14
		IO_L23P_T3_35	K2 ZBT_data6
		IO_L24N_T3_35	H5 ZBT_data19
		IO_L24P_T3_35	H6 ZBT_A2

xc7a35T CSG324 6/11

XC7A15T-2CSG324C

XC7A15T-2CSG324C

BGA_18X18_0.8MM_CENTERED

+Vdd_ZBT

U9-5

K4	VCCO_34	IO_0_34	K6 ZBT_A3
N3	VCCO_34	IO_25_34	U8 I0 IO_34_25_U8 U8 IO_34_25_U8
P6	VCCO_34	IO_L1N_T0_34	M1 ZBT_data23
T2	VCCO_34	IO_L1P_T0_34	L1 ZBT_A15
U5	VCCO_34	IO_L2N_T0_34	L3 ZBT_A19
V8	VCCO_34	IO_L2P_T0_34	K3 ZBT_data5
	1.2V-3.3V	IO_L3N_T0_DQS_34	N1 IO_34_L3n_n1 N1 IO_34_L3n
		IO_L3P_T0_DQS_34	N2 IO_34_L3p_n2 N2 IO_34_L3p
		IO_L4N_T0_34	M2 IO_34_L4n_m2 M2 IO_34_L4n
		IO_L4P_T0_34	M3 IO_34_L4p_m3 M3 IO_34_L4p
		IO_L5N_T0_34	L4 ZBT_data7
		IO_L5P_T0_34	K5 ZBT_data3
		IO_L6N_T0_VREF_34	L5 IO_34_L6n_L5 L5 IO_34_L6n
		IO_L6P_T0_34	L6 IO_34_L6p_L6 L6 IO_34_L6p
		IO_L7N_T1_34	V1 IO_34_L7N_v1 V1 (Bank34) North
		IO_L7P_T1_34	U1 IO_34_L7p_u1 U1 IO_34_L7p
		IO_L8N_T1_34	U3 IO_34_L8n_u3 U3 IO_34_L8n
		IO_L8P_T1_34	U4 IO_34_L8p_u4 U4 IO_34_L8p
		IO_L9N_T1_DQS_34	V2 IO_34_L9N_v2 V2 (Bank34) North
		IO_L9P_T1_DQS_34	U2 IO_34_L9p_u2 U2 IO_34_L9p
		IO_L10N_T1_34	V4 IO_34_L10N_v4 V4 (Bank34) North
		IO_L10P_T1_34	V5 IO_34_L10P_v5 V5 (Bank34) North
		IO_L11N_T1_SRCC_34	T3 IO_34_L11n_t3 T3 IO_34_L11n; srcc-
		IO_L11P_T1_SRCC_34	R3 IO_34_L11p_r3 R3 IO_34_L11p; srcc+
		IO_L12N_T1_MRCC_34	T4 IO_34_L12N_t4 T4 (Bank34) mrcc-
		IO_L12P_T1_MRCC_34	T5 IO_34_L12P_t5 T5 (Bank34); mrcc+
		IO_L13N_T2_MRCC_34	P5 IO_34_L13n_p5 P5 IO_34_L13n; mrcc-
		IO_L13P_T2_MRCC_34	N5 IO_34_L13p_n5 **N5 IO_34_L13p; mrcc+**
		IO_L14N_T2_SRCC_34	P3 IO_34_L14n_p3 P3 IO_34_L14n; srcc-
		IO_L14P_T2_SRCC_34	P4 IO_34_L14p_p4 P4 IO_34_L14p; srcc+
		IO_L15N_T2_DQS_34	R2 IO_34_L15n_r2 R2 IO_34_L15n
		IO_L15P_T2_DQS_34	P2 IO_34_L15p_p2 P2 IO_34_L15p
		IO_L16N_T2_34	N4 ZBT_ben_1
		IO_L16P_T2_34	M4 ZBT_ben_0
		IO_L17N_T2_34	T1 IO_34_L17n_t1 T1 IO_34_L17n
		IO_L17P_T2_34	R1 IO_34_L17p_r1 R1 IO_34_L17p
		IO_L18N_T2_34	N6 IO_34_L18n_n6 N6 IO_34_L18n
		IO_L18P_T2_34	M6 IO_34_L18p_m6 M6 IO_34_L18p
		IO_L19N_T3_VREF_34	R5 IO_34_L19n_r5 R5 IO_34_L19n
		IO_L19P_T3_34	R6 IO_34_L19p_r6 R6 IO_34_L19p
		IO_L20N_T3_34	V6 IO_34_L20N_v6 V6 (Bank34) North
		IO_L20P_T3_34	V7 IO_34_L20P_v7 V7 (Bank34) North
		IO_L21N_T3_DQS_34	V9 IO_34_L21N_v9 V9 (Bank34) North
		IO_L21P_T3_DQS_34	U9 IO_34_L21P_u9 U9 (Bank34) North
		IO_L22N_T3_34	U6 IO_34_L22N_u6 U6 (Bank34) North
		IO_L22P_T3_34	U7 IO_34_L22P_u7 U7 (Bank34) North
		IO_L23N_T3_34	T6 IO_34_L23n_t6 T6 IO_34_L23n
		IO_L23P_T3_34	R7 IO_34_L23p_r7 R7 IO_34_L23p
		IO_L24N_T3_34	T8 IO_34_L24N_t8 T8 (Bank34) North
		IO_L24P_T3_34	R8 IO_34_L24P_r8 R8 (Bank34) North

xc7a35T CSG324 5/11

XC7A15T-2CSG324C

60 wires

Byte Write Enable

ZBT_ben_[0:3]

ZBT_A[0:19]

ZBT_data[0:31]

ZBT_RW#

ZBT_adv_LD#

CLK is output to ZBT

ZBT_clk — R73 49.9 — ZBT_clk1

ZBT_clk — R76 49.9 — ZBT_clk2

0201

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

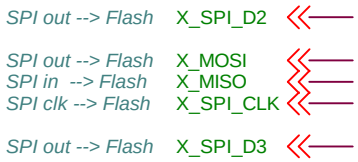
GND

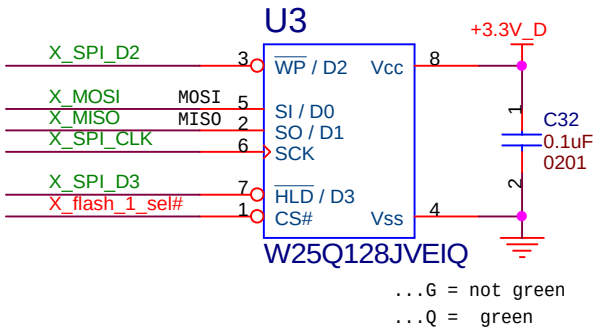
Title	Artix banks 34 and 35		
Size: Custom	Document Number: A - RiskFive Artix Bone With ZBT Memory		Rev: 0
Date: Friday, July 20, 2018		Sheet 5 of 29	

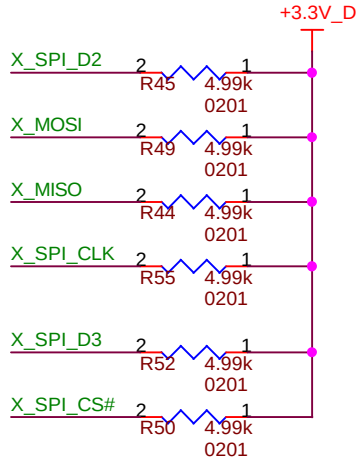
Artix configuration SPI flash and Solid State Disk

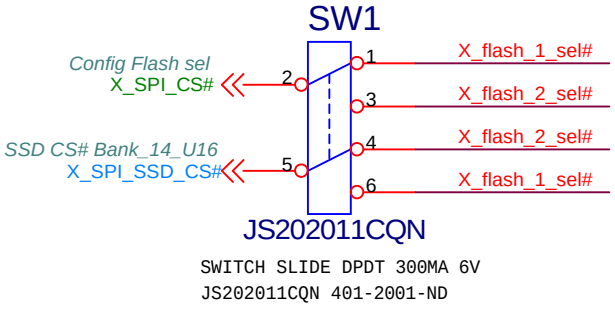
Two possible use cases:
1) Dual boot.
2) Boot and SSD.

SPI CLK is the same pin as Configuration CCLK. It can be used after configuration via STARTUP2 "primitive" described in UG470 v1.8 page 94. On this board I also routed pin L16 (L6P_EMCCLK) to the same CCLK. The "primitive" is not necessary.

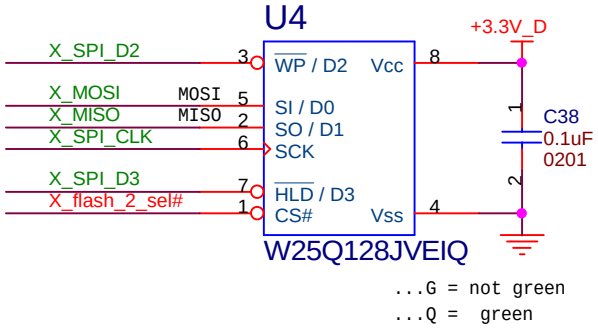








Compatible 8x6 parts
SO-8 W25Q128JVSI
WSON W25Q128JVEI



SOG.050/8/WG.300/L.250
WINBOND_WSON8_8X6MM

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

GND

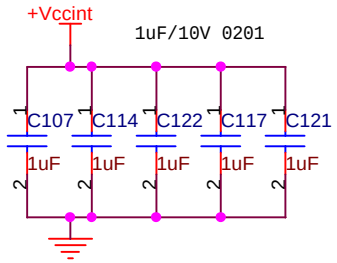
SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

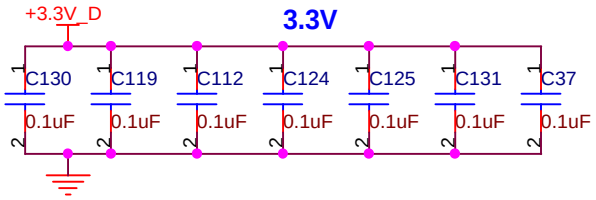
Page Contents
SPI configuration flash

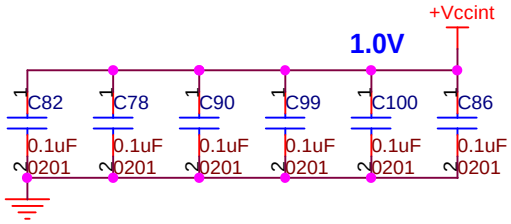
Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

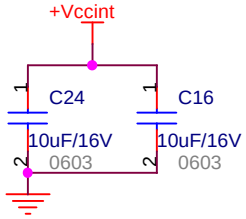
Date: Friday, July 20, 2018 Sheet 6 of 29

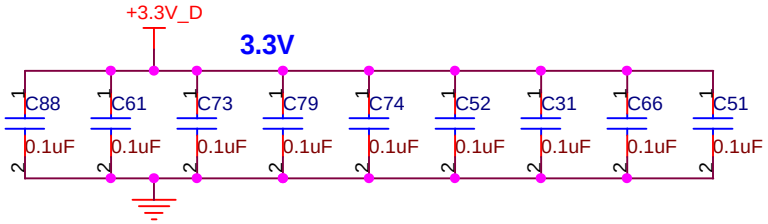
FPGA power filtering

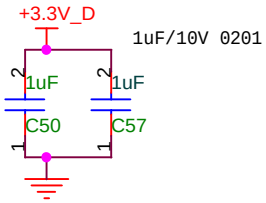


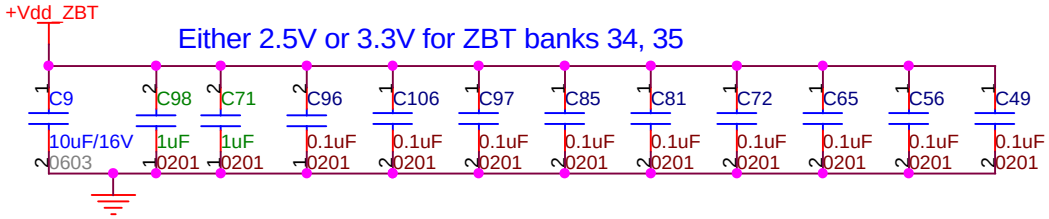


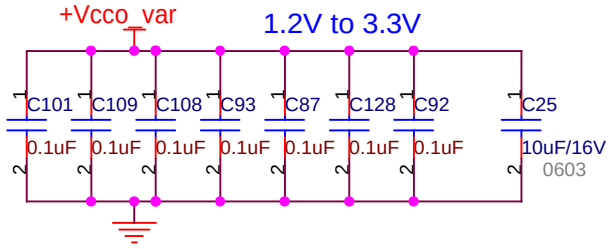












07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents: FPGA decoupling

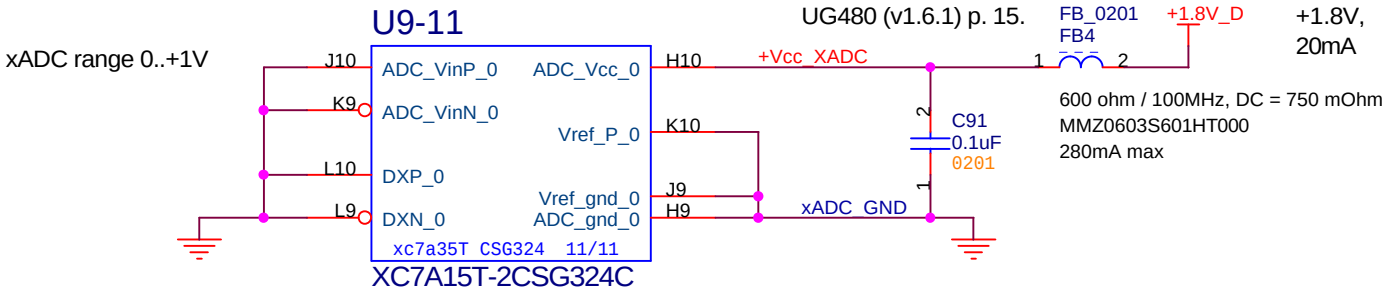
Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 7 of 29

Artix xADC

Powering and using xADC: see UG480 (v1.6.1) p. 77.

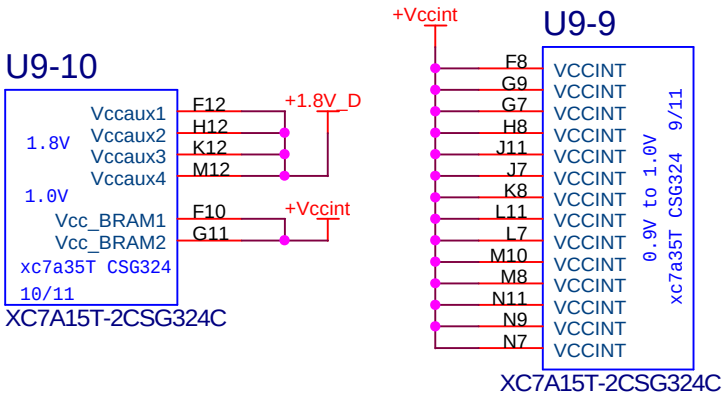
P.14: xADC internal schematics and on-die sensors.
P.15: How to connect xADC pins.

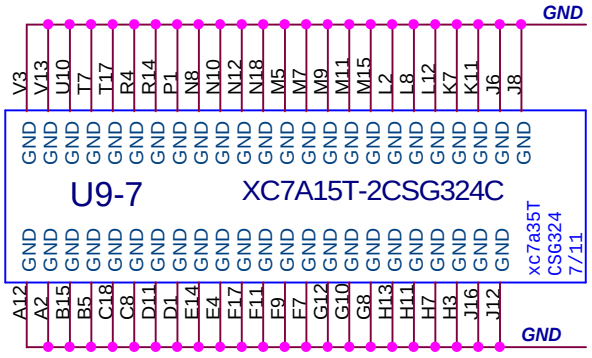


XC7A15T-2CSG324C

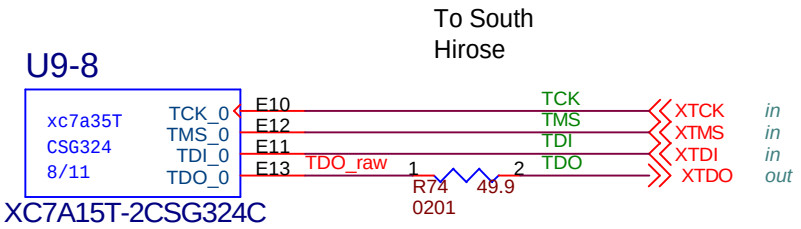
BGA_18X18_0.8MM_CENTERED

Artix GND, VccAUX, VccBRAM, and Vccint





Artix JTAG



07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents: Artix JTAG, xADC, GND, VccAUX, VccBRAM, and Vccint

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 8 of 29

Gigabit PHY

SGMII = 4 wires

Rx data to MAC SGMII_from_PHY- RXD3
Rx data to MAC SGMII_from_PHY+ RXD2

Tx data from MAC SGMII_to_PHY+ TXD1
Tx data from MAC SGMII_to_PHY- TXD0

Mngmnt data SGMII_MDIO_DATA MDIO
Mngmnt clock SGMII_MDIO_CLK MDC

To processor SGMII_interrupt PHY_interrupt

Synch Ethernet recovered clock

125MHz SGMII_Synch_CLK 2 49.9 R72 0201 1 CLK_125_raw

U8D

+1.8V

PHY is making its own 1.8V to avoid sequencing.

Avdd_1v8 13, 48
Either in or NC
TMS 22
TDI 23
TDO 21
TCK 20
+3.3V_D

Avdd_2v5 3, 9 ~200 mA +2.5V_D
3.3V Vddo 19 +3.3V_D
2.5V Vddo 30
1.8V Vddo 41 +1.0V_PHY
PHY_Vdd10 6
DVdd_1v0 24, 31, 42 Max 1.155V ~100 mA

DP83867 GbE PHY 4/4

DP83867CSRGZT

U8C DP83867CSRGZT

DP83867 GbE PHY 3/4

LED0 pin strapping
Mode 1 mirror - SGMII -
Mode 2 mirror - SGMII +
Mode 3 mirror + SGMII -
Mode 4 mirror + SGMII +

gnd49 49, gnd50 50, gnd51 51, gnd52 52, gnd53 53, gnd54 54, gnd55 55, gnd56 56, gnd57 57, gnd58 58, gnd59 59, gnd60 60, gnd61 61

+1.8V_D
C95 0.1uF

+2.5V

U6

+3.3V_D 1, 3
Vin Vout 5
en
TLV700xx
LDO 200mA
SOT23 DDC
SC70 DCK
gnd nc 4
2
~200 mA +2.5V_D
C80 1uF 0201

TLV70025DCK

LDO is stable with 0.1uF, but 1uF is recommended. TLV70028DCKR or -T.

+1.0V; 110mA

+1.0V_PHY PHY_Vdd10 FB5 220/2A +Vccint

PHY in QFN package requires 1.0V

Power sequence requirements when 1.8V is not provided: NONE.

Mirrored; D.S. page 35
A . D 0 -> 3
B . C 1 -> 2
C . B 2 -> 1
D . A 3 -> 0

HIGH = FPGA configured
LOW = not configured

From FPGA X_DONE
CLK_25MHz_1V8 Ethernet PHY clock

U8B

reset 43
xtal_in_1.8V 15
25 MHz
1.8V
xtal_out_1.8V 14
intrpt_pdwn 44
LED3 or PTP
GPIO_0 39
GPIO_1 40
Rbias_11.0k 12
DP83867 GbE PHY 2/4

DP83867CSRGZT

R62 4.99k 0201
PHY_interrupt
PHY_GPIO_0
PHY_GPIO_1
PHY_bias
R71 11.0k 0201

PTP Start_Frame
R64 11.0k 0201

Do we need to mirror? It depends on the motherboard.

SGMII can be implemented in 3.3V bank. LVDS reception works for any Vcco with external termination. (Internal termination requires 2.5V.). LVDS transmission requires 2.5V, but TMDS can be used at any Vcco.

DP83867CSRGZ = PHY with RGMII/SGMII
DP83867CRRGZ = PHY with RGMII only
They are pin compatible

Ports are "mirrored" in reverse order.
A --> 3, B --> 2, etc.

Center tap to AVdd not required. Internal on-chip termination provided on Media Dependent Interface (i.e., magnetics).

PTP stamps are on GPIO pins
D.S. Page 88.

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Compgroup 97

Mode	Rlo	Rhi (p.36)
1	open	open
2	2.49k	10.0k
3	2.49k	5.76k
4	open	2.49k

PHY configuration using strap resistors.
Rx_D0, D2: Mode 1 --> addr = 0
Rx_CTRL: Mode 3 --> auto negotiate.
LED0: Mode 1 --> RGMII w/o mirror.
LED0: Mode 2 --> SGMII w/o mirror.
LED0: Mode 3 --> RGMII with mirror.
LED0: Mode 4 --> SGMII with mirror.

R16 2.49k 0201 Rx_CTRL R17 5.76k 0201 +3.3V_D Mode 3

R14 DNP 0201 PHY_LED0 R15 2.49k 0201 +3.3V_D Mode 4
DNP 2.49k Mode 4 -> SGMII

SGMII MDIO diagnostics

J2
MDC 1
GND 2
MDIO 3
GND 4
Header 4 pins

U8A QFN-48

FPGA from PHY: LVDS_25 in

RGMII SGMII RJ45

RXD2 0.1uF C12
RXD3 0.1uF C11
RXD0_SG_clk+ 33
RXD1_SG_clk- 34
RXD2_SG_out+ 35
RXD3_SG_out- 36
opt
mdi0_p 1 Ether3+ 11
mdi0_n 2 Ether3- 11

Rx_CTRL
RX_CLK_out 32
RX_CTRL_out 38
mdi1_p 4 Ether2+ 11
mdi1_n 5 Ether2- 11

TXD0 0.1uF C13
TXD1 0.1uF C14
TXD0_SG_in- 28
TXD1_SG_in+ 27
TXD2 26
TXD3 25
mdi2_p 7 Ether1+ 11
mdi2_n 8 Ether1- 11

FPGA to PHY: TMDS_33 out

TX_CLK_in 29
TX_CTRL_in 37
mdi3_p 10 Ether0+ 11
mdi3_n 11 Ether0- 11

terminated 100 ohm

CLK_125_raw
CLK125_out 18

Activity Ether_LED1 PHY_LED2 45 LED2
1000 link PHY_LED1 46 LED1
Link Ether_LED0 PHY_LED0 47 LED0

MDC 16
MDIO 17

R19 2k 0201 +3.3V_D R18 2k 0201

DP83867 GbE PHY 1/4

DP83867CSRGZT

MDIO fmax = 25 MHz

GND

Footprint 0402_CA
PHY_LED1 LEDg LED4 A C R10 2k 0201
0402 straight up
PHY_GPIO_1 LEDg LED5 A C R11 2k 0201
0402 straight up

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents: GbE PHY

Size	Document Number	Rev
Custom	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 9 of 29

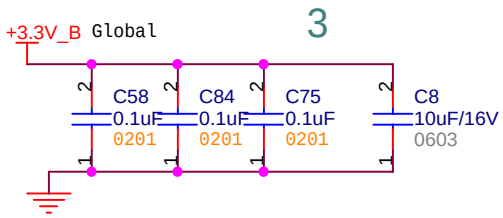
Texas Instruments PHY

In addition to usual PHY duties, the PHY is supposed to:

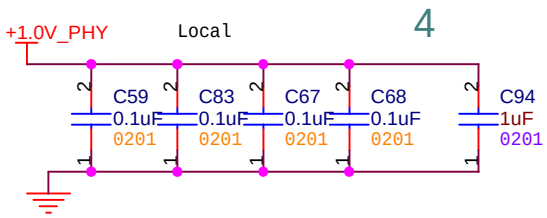
1. Recover the 125 MHz clock from Synchronous Ethernet.

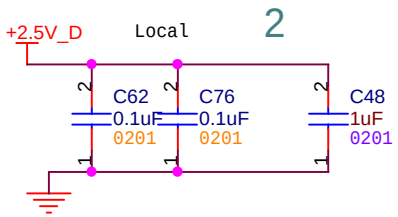
2. Present the 125 MHz clock to the FPGA.

3. The PHY makes its own 1.8V voltage rail w/o decoupling.



Group 97





07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
GbE PHY decoupling

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 10 of 29

0603
10 uF C1608X5R1A106K

0402
10 nF TMK105B7103KV-F
0.1uF C1005X5R1E104K, M
1uF C1005X5R1A105K or M
4.7uF CL05A475MP5NRNC

CAP CER 0.1UF 16V 10% X5R 0201
C0603X5R1C104K030BC TDK

NORTH header

Bank 34 = 3.3V or 2.5V
Bank 0 = 3.3V
Bank 14 = 3.3V
Banks 15,16: Vcco_var

JH1A

	DOWN inside brd			UP outside brd	
	K18 (Bank 14) XSPI_miso	1	80	POWER_ON	HIGH to Enable 3.3V power
	K17 (Bank 14) XSPI_mosi	2	79	X_PRGM#	P9 FPGA conf (Bank 0)
	L14 (Bank 14) XSPI_D2	3	78	X_DONE	P10 FPGA conf (Bank 0)
	M14 (Bank 14) XSPI_D3	4	77	IO_15_L23P_j17	J17 (Bank 15)
	E9 & L16 (Bank 0 & 14) XSPI_CCLK	5	76	IO_15_L23N_j18	J18 (Bank 15)
	U14 (Bank 14) IO_14_L22P_u14	6	75	IO_15_0_g13	G13 (Bank 15, SE)
	V14 (Bank 14) IO_14_L22N_v14	7	74	IO_14_L15P_r16	R16 (Bank 14)
	T13 (Bank 14) IO_14_L23P_t13	8	73	IO_14_L15N_t16	T16 (Bank 14)
	U13 (Bank 14) IO_14_L23N_u13	9	72	IO_14_L14P_t14	T14 Bank_14_SRCC
	U12 (Bank 14) IO_14_L20P_u12	10	71	IO_14_L14N_t15	T15 Bank_14_SRCC
	V12 (Bank 14) IO_14_L20N_v12	11	70	IO_14_L8P_n14	N14 (Bank 14)
	R12 (Bank 14) IO_14_L5P_r12	12	69	IO_14_L8N_p14	P14 (Bank 14)
	R13 (Bank 14) IO_14_L5N_r13	13	68	SRST	
	T11 (Bank 14) IO_14_L19P_t11	14	67	IO_14_0_r11	R11 (Bank 14) sngl (SW reset)
	U11 (Bank 14) IO_14_L19N_u11	15	66	IO_14_L24P_t9	T9 (Bank 14)
	V10 (Bank 14) IO_14_L21P_v10	16	65	IO_14_L24N_t10	T10 (Bank 14)
	V11 (Bank 14) IO_14_L21N_v11	17	64	IO_34_L21P_u9	U9 (Bank34)
	R10 (Bank 14) sngl IO_14_25_r10	18	63	IO_34_L21N_v9	V9 (Bank34)
	R8 (Bank34) IO_34_L24P_r8	19	62	IO_34_25_U8	U8 IO_34_25_U8
	T8 (Bank34) IO_34_L24N_t8	20	61	IO_34_L23p_r7	R7 IO_34_L23p
	V7 (Bank34) IO_34_L20P_v7	21	60	IO_34_L23n_t6	T6 IO_34_L23n
	V6 (Bank34) IO_34_L20N_v6	22	59	IO_34_L22P_u7	U7 (Bank34)
	R6 IO_34_L19p IO_34_L19p_r6	23	58	IO_34_L22N_u6	U6 (Bank34)
	R5 IO_34_L19n IO_34_L19n_r5	24	57	IO_34_L13p_n5	N5 IO_34_L13p; mrcc+
	V5 (Bank34) IO_34_L10P_v5	25	56	IO_34_L13n_p5	P5 IO_34_L13n; mrcc-
	V4 (Bank34) IO_34_L10N_v4	26	55	IO_34_L8p_u4	U4 IO_L8p_T1_34
	T5 (Bank 34) mrcc+ IO_34_L12P_t5	27	54	IO_34_L8n_u3	U3 IO_L8n_T1_34
	T4 (Bank 34) mrcc- IO_34_L12N_t4	28	53	IO_34_L6p_L6	L6 IO_34_L6p
	R3 IO_L11p_T1_34; srcc+ IO_34_L11p_r3	29	52	IO_34_L6n_L5	L5 IO_34_L6n
	T3 IO_L11n_T1_34; srcc- IO_34_L11n_t3	30	51	IO_34_L14p_p4	P4 IO_34_L14p; srcc+
	U2 IO_L9p_T1_34 IO_34_L9p_u2	31	50	IO_34_L14n_p3	P3 IO_34_L14n; srcc-
	V2 IO_34_L9N_v2 IO_34_L9N_v2	32	49	IO_34_L15p_p2	P2 IO_34_L15p
	U1 IO_L7p_T1_34 IO_34_L7p_u1	33	48	IO_34_L15n_r2	R2 IO_34_L15n
	V1 IO_34_L7n_v1 IO_34_L7n_v1	34	47	IO_34_L17p_r1	R1 IO_34_L17p
	M6 IO_34_L18p IO_34_L18p_m6	35	46	IO_34_L17n_t1	T1 IO_L17n_T2_34
	N6 IO_34_L18n IO_34_L18n_n6	36	45	IO_16_L19N_d10	D10 (Bank 16)
	N2 IO_34_L3p IO_34_L3p_n2	37	44	IO_16_L6N_d9	D9 (Bank 16)
	N1 IO_34_L3n IO_34_L3n_n1	38	43	IO_16_L11P_c9	C9 (Bank 16) srcc+
	M3 IO_34_L4p IO_34_L4p_m3	39	42	IO_16_L11N_b9	B9 (Bank 16) srcc-
	M2 IO_34_L4n IO_34_L4n_m2	40	41	IO_16_L12P_b8	B8 (Bank 16) mrcc+
				IO_16_L12N_a8	A8 (Bank 16) mrcc-

Bank 15 var
Bank 14 3.3V
Bank 34 3.3V
Bank 16 var

FX11LA-80P/8-SV(71)

Footprint FX11L80/H/GP

JH1B NORTH

sh1	sh1	END1	END1
sh2	sh2	END2	END2
sh3	sh3	sh8	sh8
sh4	sh4	sh7	sh7
sh5	sh5	sh6	sh6
Post1	Post1	Post2	Post2

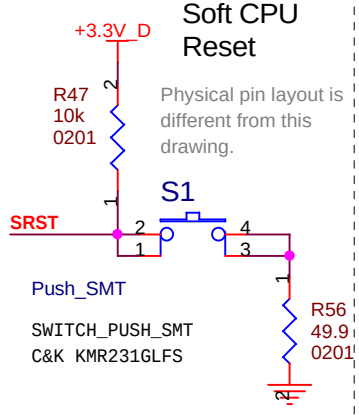
FX11LA-80P/8-SV(71)

CONN HEADER 80POS W/POSTS SMD
FX11LA-80P/8-SV(71) -> mezzanine

CONN RECEPT 80POS W/POSTS SMD
FX11LA-80S/8-SV(71) -> motherboard

GND

Soft CPU Reset



Physical pin layout is different from this drawing.

This pushbutton can be used for anything. Its intended use is restarting the soft CPU operating system.

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

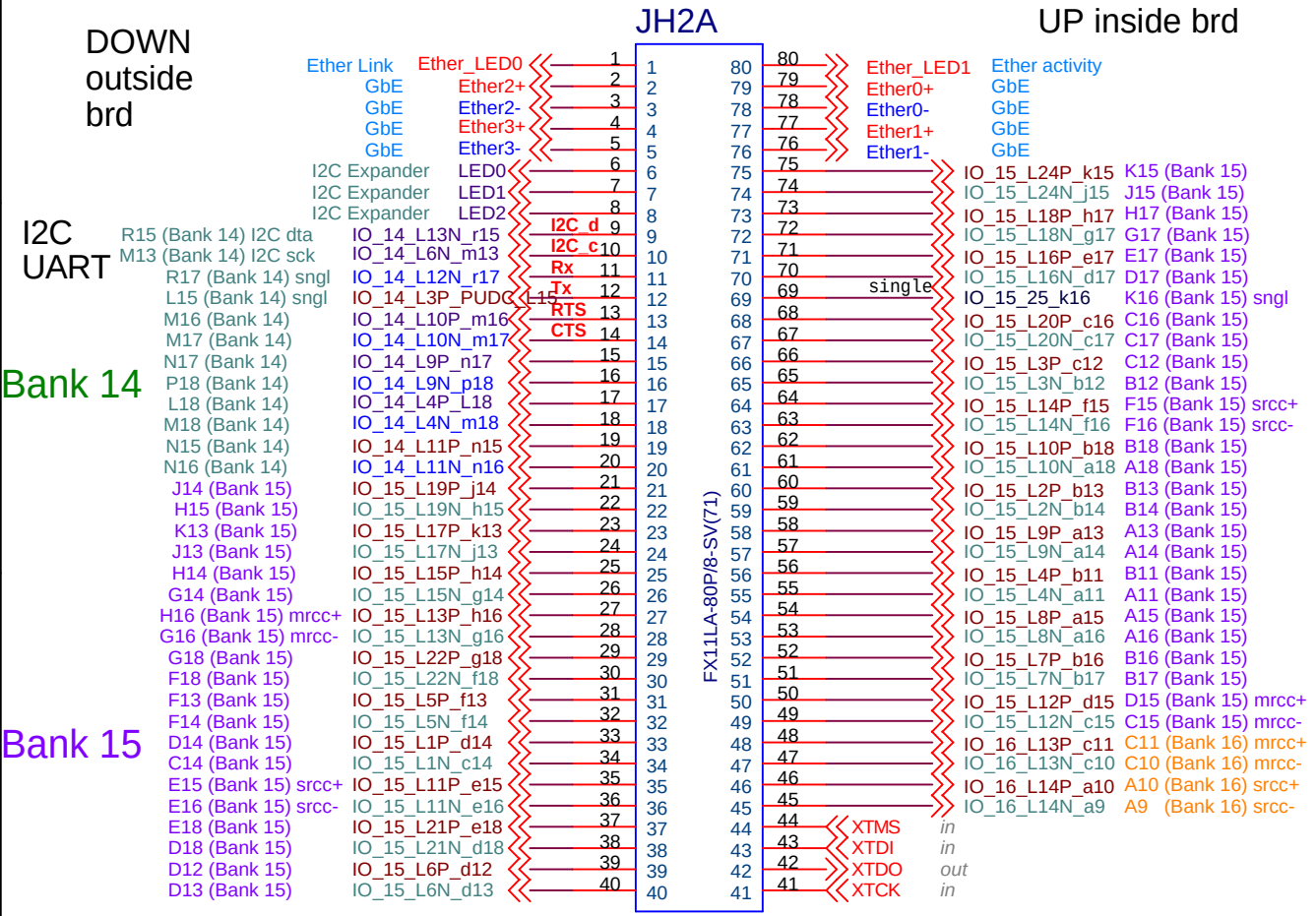
Page Contents: High density Hirose connectors

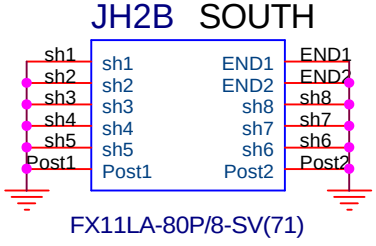
Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 11 of 29

SOUTH header

FTDI cable with 450mA +5V power
USB --> JTAG, UART
FTDI part C232HD-EDHSP-0

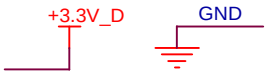




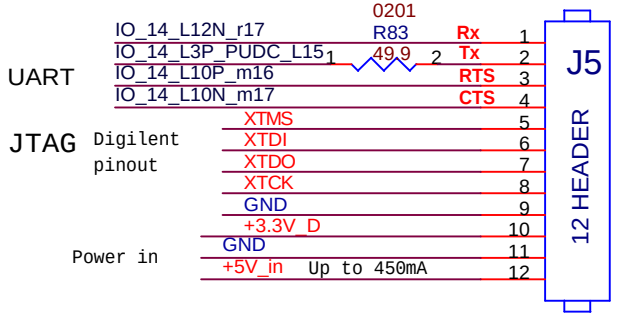
Footprint FX11L80/H/GP

CONN HEADER 80POS W/POSTS SMD
FX11LA-80P/8-SV(71) -> daughter card

CONN RECEPT 80POS W/POSTS SMD
FX11LA-80S/8-SV(71) -> motherboard



East

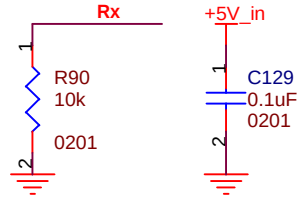


Bank 15

West

UART pulldown(s)
PUDC has one elsewhere

Bank 16



07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
High density Hirose connectors

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

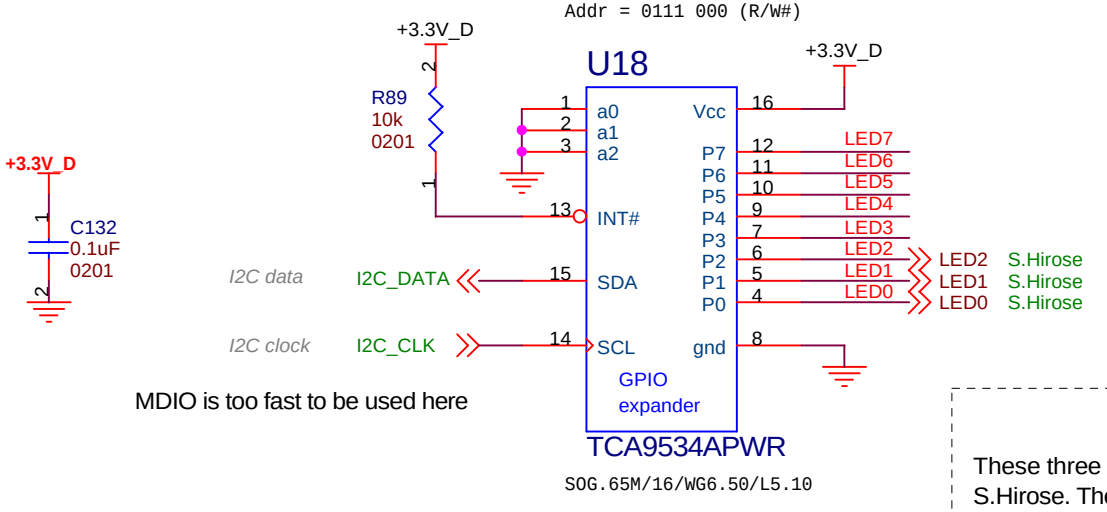
Date: Friday, July 20, 2018 Sheet 12 of 29

I2C Expander and I2C temp sensor

There were not enough pins to connect the LEDs directly to the FPGA

Expander slave address 0111 a2 a1 a0 (R/W#)
Push-pull output structure on P0..P7.
Max freq 400 kHz

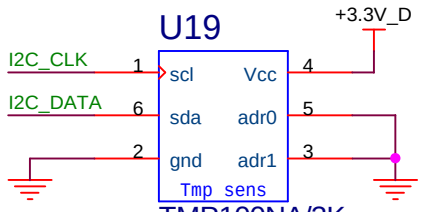
Addr = 0111 000 (R/W#)



MDIO is too fast to be used here

SOG.65M/16/WG6.50/L5.10

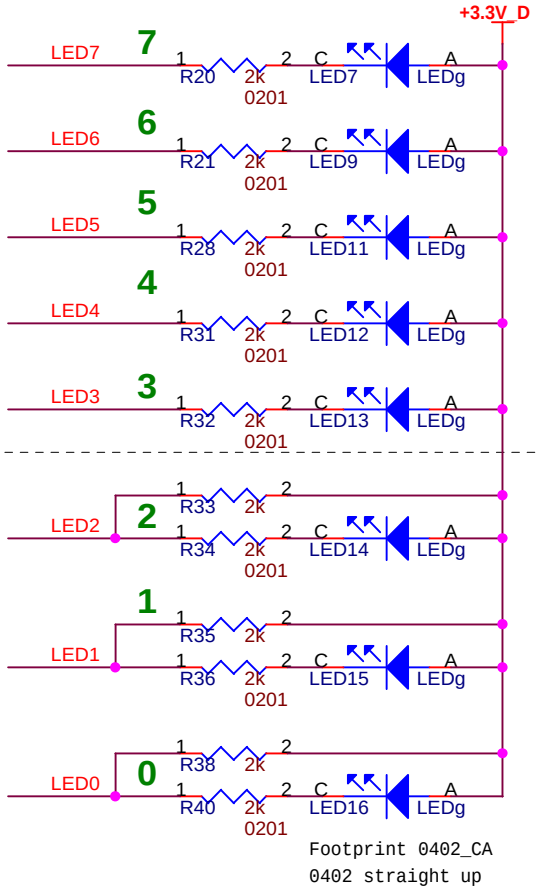
Addr = 1001 000 (R/W#)



The temp sensor is meant for measuring the temperature and also for I2C development. It is less expensive than the ADT7420 from Chu's book.

TMP100 temp sensor I2C
TMP100NA/3K
SOT-23-6PADS

Status LED's Active LOW



These three are connected to S.Hirose. They can be used as chip select pins on the motherboard. The pullups provide a well defined HIGH default.

Footprint 0402_CA
0402 straight up

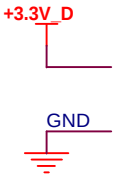
0603 up

LTST-C190TGKT	grn bright
LTST-C190KGKT	grn dim
LTST-C190KSKT	yellow
LTST-C190KFKT	orange
LTST-C190KRKT	red
LTST-C190KAKT	red
LTST-C190TBKT	blue

0402 up

APHHS1005CGCK	grn	40 mcd
APHHS1005SYCK	yllw	150 mcd
APHHS1005SECK	orng	150 mcd
APHHS1005SURCK	red	70 mcd
APHHS1005QBC/D	blue	60 mcd

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.



Group 99

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

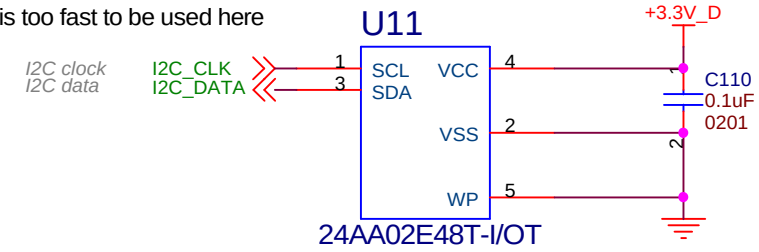
Page Contents
Diagnostic LEDs

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	1

Date: Friday, July 20, 2018 Sheet 13 of 29

MAC ID EEPROM
400 kHz

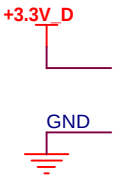
MDIO is too fast to be used here



WP pin is n.c. in this part

MAC ID EPPROM on I2C0
Plastic SOT-23, 5-lead
Address = 1010 000

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.



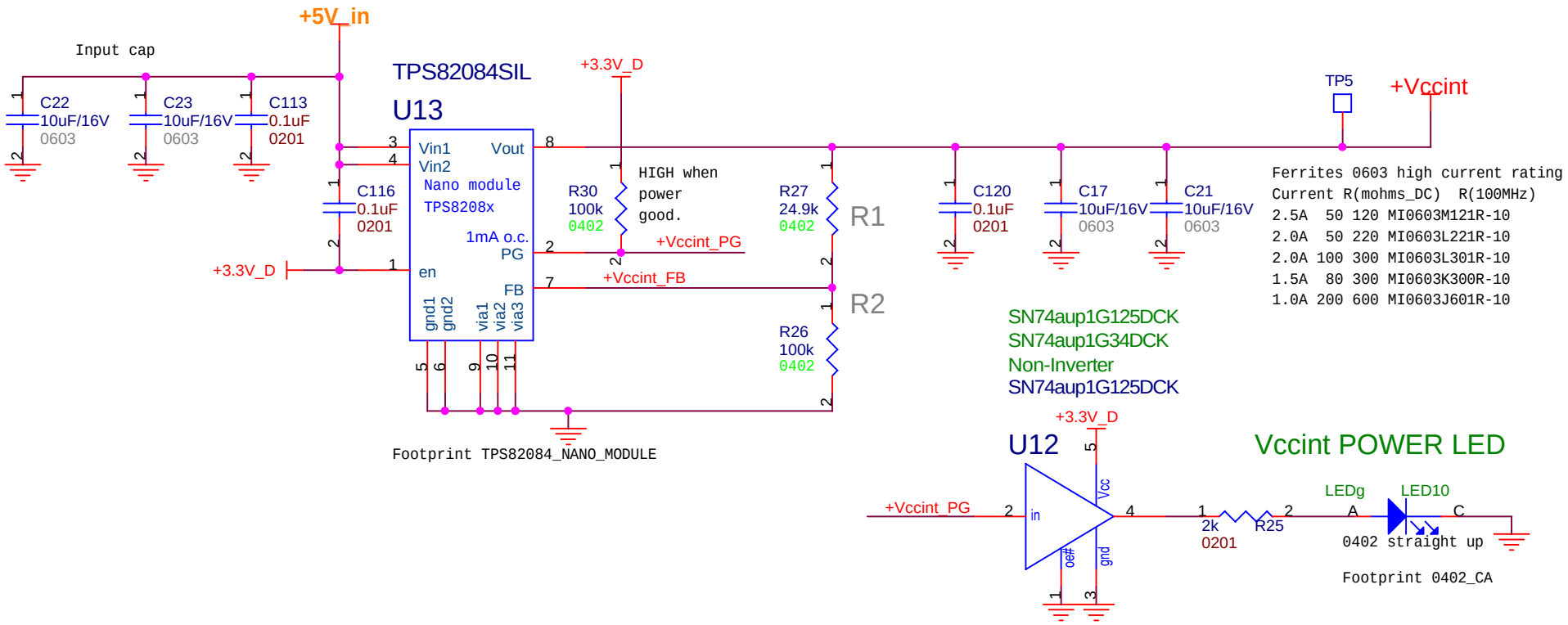
SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
MAC ID EEPROM

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	1

Date: Friday, July 20, 2018 Sheet 14 of 29

1.00V for Vccint



SC-70 with 5 pins;
push-pull

TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
Vout = 1.00V --> R1 = 25.00k
Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
```

Need five positive voltages.
1.35V or 1.5V for DDR3L
1.8_D for FPGA & HDMI
1.0V_D for FPGA
3.3V_D for logic
Variable Vcco

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
TPS82084SIL   $3.11  2 A *
TPS82085SIL   $4.05  3 A *
```

07/14/2018. PRELIMINARY
prototype release for review.
Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

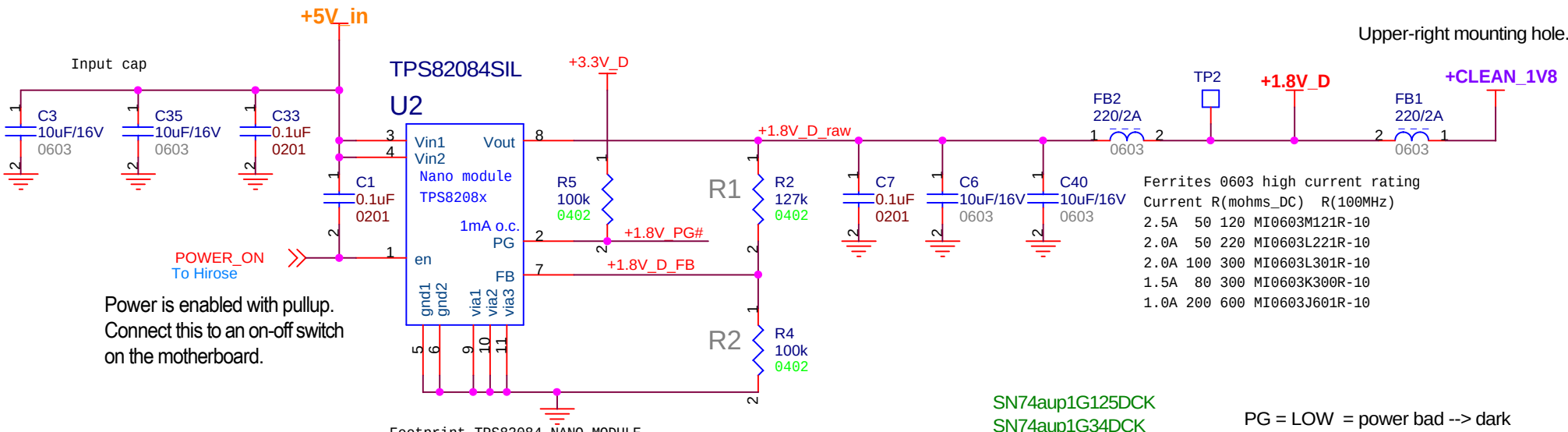
Page Contents
+1.35V DC/DC generator for DDR3L

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 15 of 29

1.8V for FPGA VccAUX and for the external chips

This voltage is also delivered on a upper-right mounting hole.

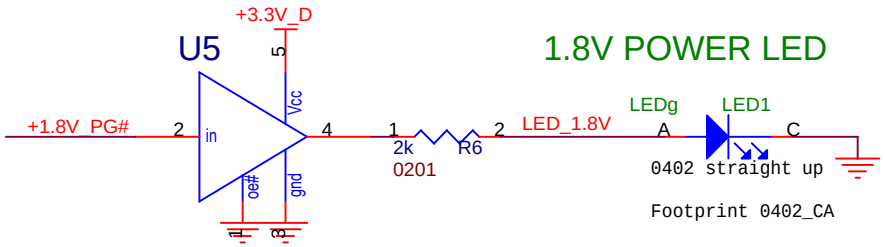


Power is enabled with pullup.
Connect this to an on-off switch
on the motherboard.

Footprint TPS82084_NANO_MODULE

SN74aup1G125DCK
SN74aup1G34DCK
Non-Inverter
SN74aup1G125DCK

PG = LOW = power bad --> dark
PG = HIGH = power good--> glow



1.8V POWER LED

SC-70 with 5 pins;
push-pull

TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
Vout = 1.00V --> R1 = 25.00k
Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.77V --> R1 = 121.0k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
```

Need five positive voltages.
1.35V or 1.5V for DDR3L
1.8_D for FPGA & HDMI
1.0V_D for FPGA
3.3V_D for logic
Variable Vcco

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
TPS82084SIL    $3.11  2 A *
TPS82085SIL    $4.05  3 A *
```

07/14/2018. PRELIMINARY
prototype release for review.
Not manufactured yet.

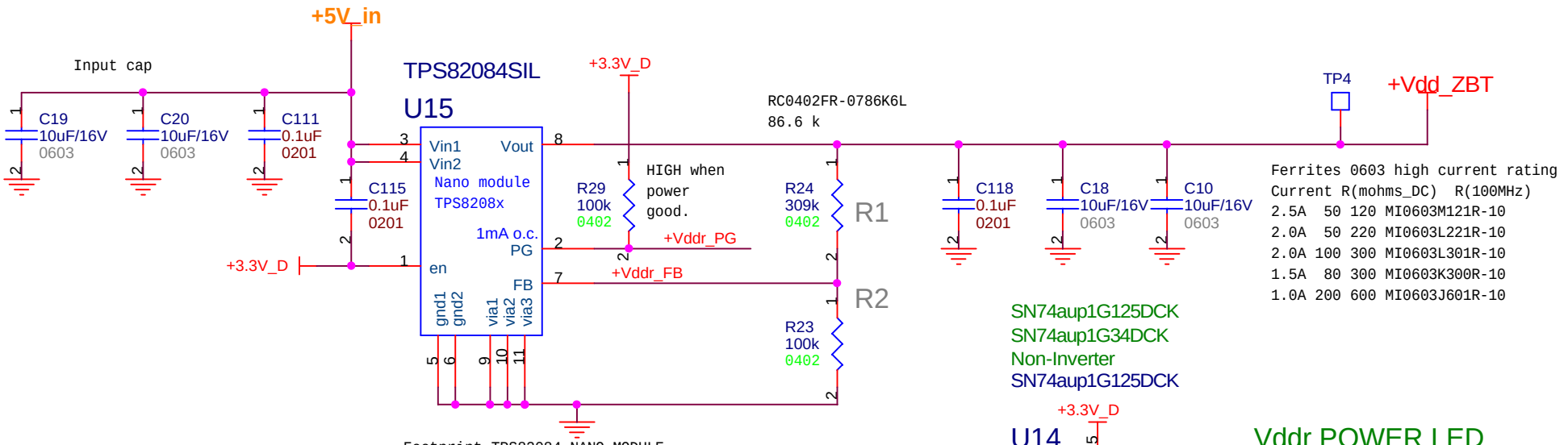
SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
+1.8V DC/DC generator for VccAUX, HDMI chip, and for the motherboard

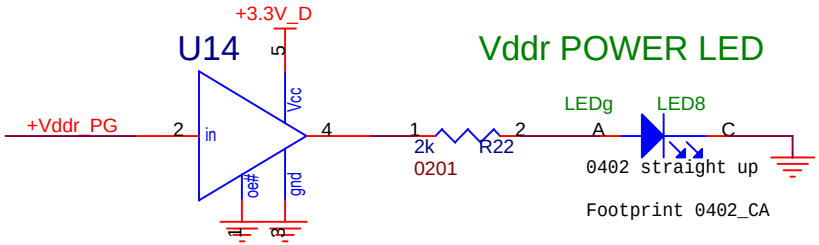
Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 16 of 29

Either 3.3V or 2.5V for ZBT chips and banks 34, 35.
Use 2.5V if the banks use LVDS, and also change
the ZBT chip.



SN74aup1G125DCK
SN74aup1G34DCK
Non-Inverter
SN74aup1G125DCK



SC-70 with 5 pins;
push-pull

07/14/2018. PRELIMINARY
prototype release for review.
Not manufactured yet.

TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
Vout = 1.00V --> R1 = 25.00k
Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 86.6 k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
```

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
TPS82084SIL    $3.11  2 A *
TPS82085SIL    $4.05  3 A *
```

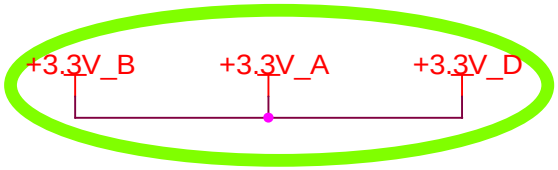
SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

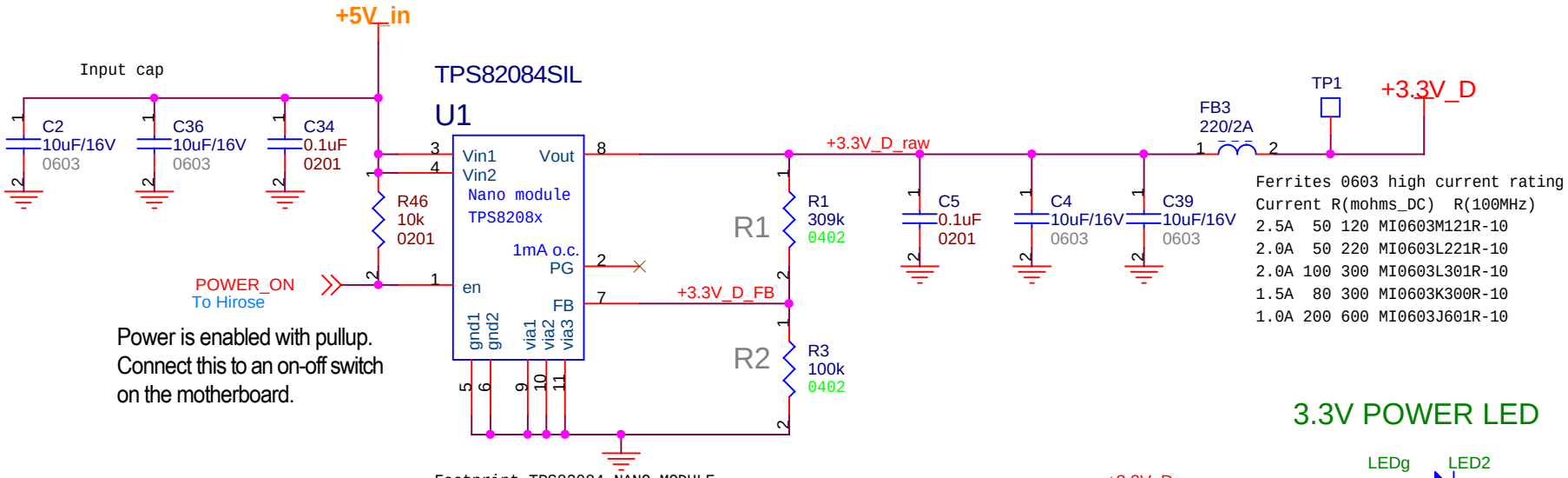
Page Contents
+1.35V DC/DC generator for DDR3L

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 17 of 29

3.3V for all on-board circuits.

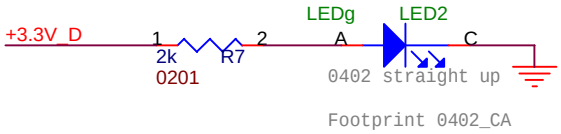




Power is enabled with pullup.
Connect this to an on-off switch
on the motherboard.

```
Ferrites 0603 high current rating
Current R(mohms_DC)  R(100MHz)
2.5A  50 120 MI0603M121R-10
2.0A  50 220 MI0603L221R-10
2.0A 100 300 MI0603L301R-10
1.5A  80 300 MI0603K300R-10
1.0A 200 600 MI0603J601R-10
```

3.3V POWER LED



TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
Vout = 1.00V --> R1 = 25.00k
Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
```

Need five positive voltages.
1.35V or 1.5V for DDR3L
1.8_D for FPGA & HDMI
1.0V_D for FPGA
3.3V_D for logic
Variable Vcco

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
TPS82084SIL   $3.11  2 A *
TPS82085SIL   $4.05  3 A *
```

07/14/2018. PRELIMINARY
prototype release for review.
Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
+3.3V DC/DC generator for most of the board

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

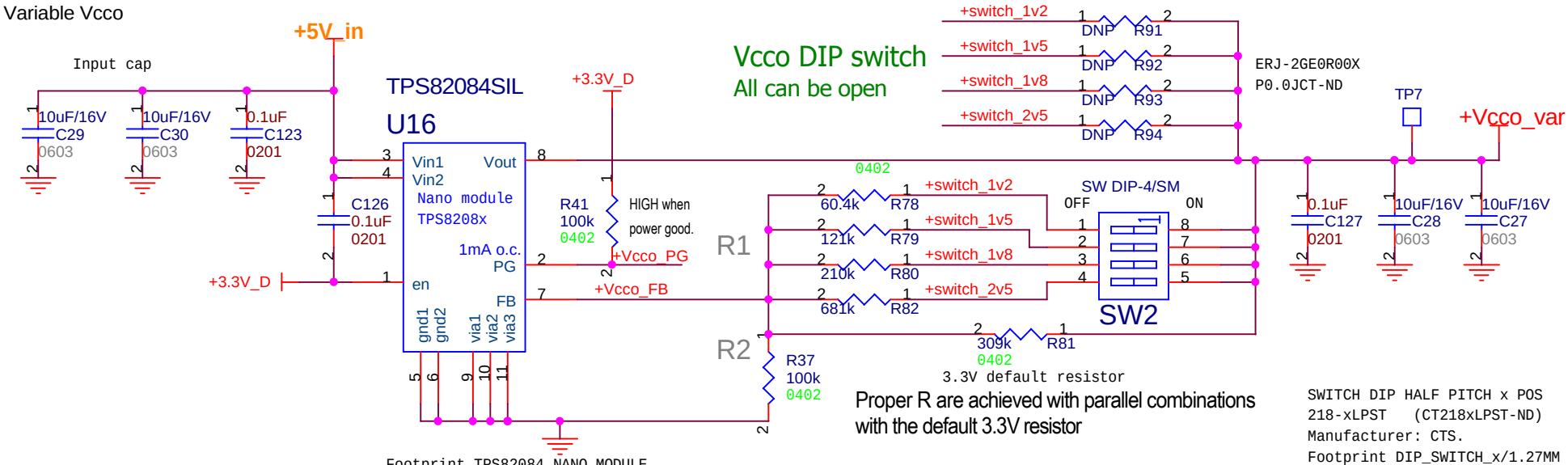
Date: Friday, July 20, 2018 Sheet 18 of 29

Variable Vcco for South Hirose banks 15, 16

Need five positive voltages.
1.35V or 1.5V for DDR3L
1.8_D for FPGA & HDMI
1.0V_D for FPGA
3.3V_D for logic
Variable Vcco

When all switches are OFF --> select 3.3V
Other voltages selected with switches

For fixed voltage install one of these
zero-ohm and do not install the switch.

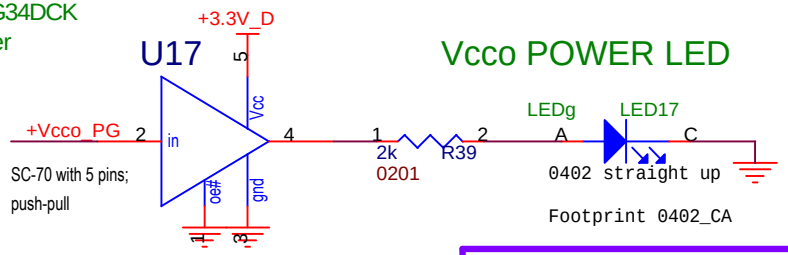


Proper R are achieved with parallel combinations with the default 3.3V resistor

SWITCH DIP HALF PITCH x POS
218-xLPST (CT218xLPST-ND)
Manufacturer: CTS.
Footprint DIP_SWITCH_x/1.27MM
x = 4 or 6 (3 & 5 not avail).

SN74aup1G125DCK
SN74aup1G34DCK
Non-Inverter

SN74aup1G125DCK



Vcco POWER LED

```
1.20V --  60.4k RC0402FR-0760K4L
1.50V --   121k RC0402FR-07121KL
1.80V --   210k RC0402FR-07210KL
2.50V --   681k RC0402FR-07681KL
All OFF --> default 3.3V
3.30V --   309k RC0402FR-07309KL
```

```
1.2V --> 1/x = 1/50.00 - 1/309 --> x =  59.7 --> R=60.4k
1.5V --> 1/x = 1/87.50 - 1/309 --> x = 122.1 --> R=121k
1.8V --> 1/x = 1/125.0 - 1/309 --> x = 209.9 --> R=210k
2.5V --> 1/x = 1/212.5 - 1/309 --> x = 680.4 --> R=681k
```

```
Vout = 1.00V --> R1 = 25.00k
Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
Use DIP switch
```

TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
TPS82084SIL    $3.11   2 A *
TPS82085SIL    $4.05   3 A *
```

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
Variable Vcco for South Hirose banks 15, 16

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 19 of 29

Power network names and power entry

Alter ego

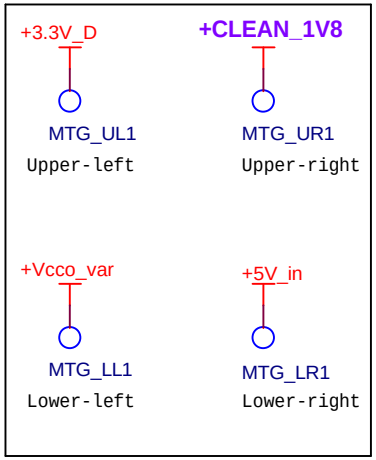
+3.3V_A +3.3V_B +3.3V_D

Two banks with variable Vcco 1.2V to 3.3V

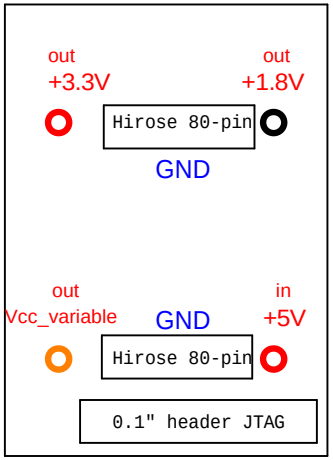
+Vcco_var

C26
10uF/16V
0603

Powered mounting holes



Board sketch



The board is powered with the lower-right mounting hole. Three other mounting holes are power outputs.

Hirose shields are ground.

TP3 TP6

07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

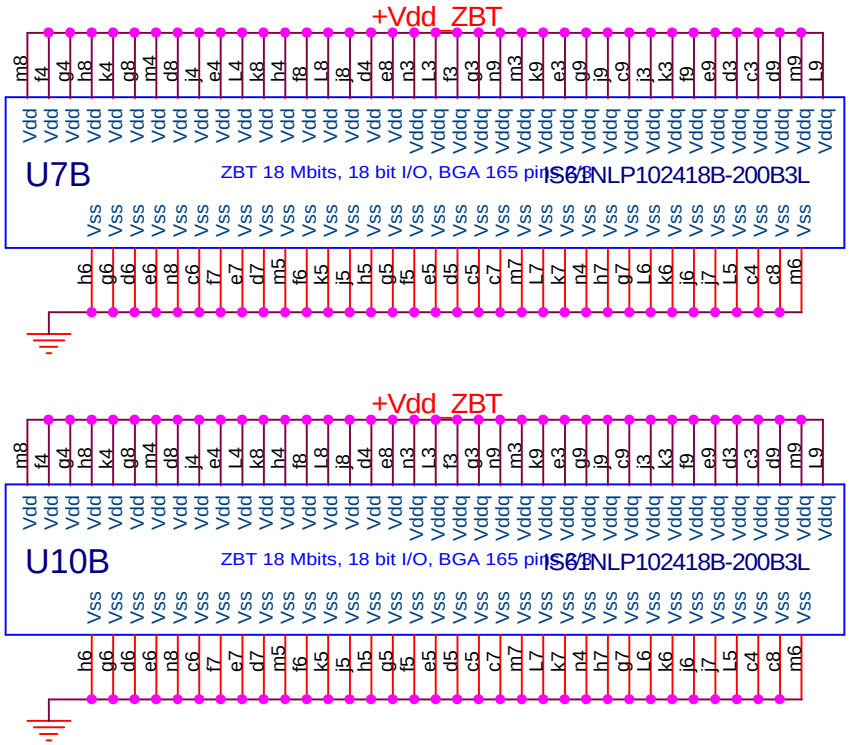
Page Contents
Power network names and power entry

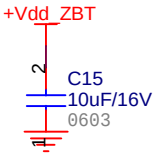
Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

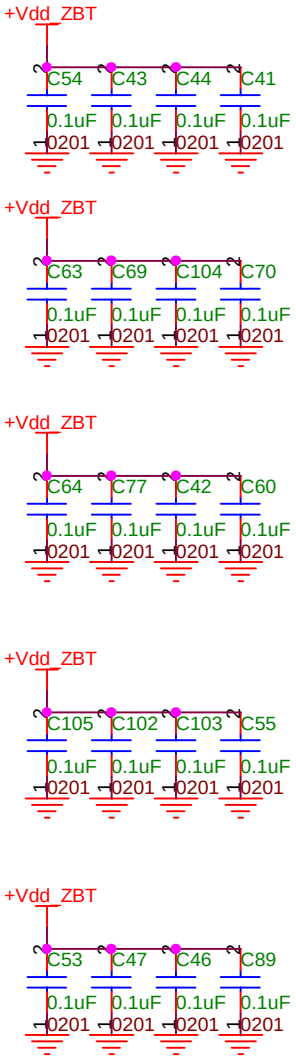
Date: Friday, July 20, 2018 Sheet 20 of 29

ZBT SRAM 1024k * 36 bits

Manufacturer Part Number
IS61NLP102418B
SRAM 18 MBIT
200MHZ 165 BGA
706-1388-ND $19.31/ea
D-K: 103 on 03/01/2018







07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Group 30

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
ZBT SRAM

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 21 of 29

ZBT SRAM 1024k * 36 bits

Footprint X_BGA165_1mm

Manufacturer Part Number
IS61NLP102418B
SRAM 18 MBIT
200MHZ 165 BGA
706-1388-ND $19.31/ea
D-K: 103 on 03/01/2018

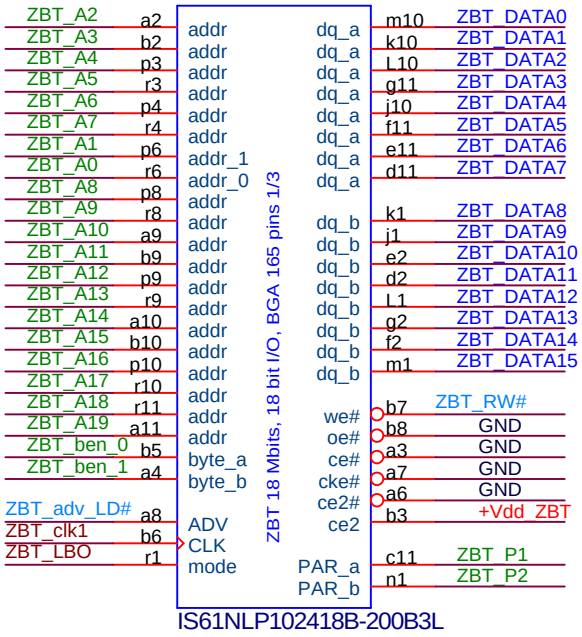
OE# is mentioned
Data Sheet p.13
Can be grounded

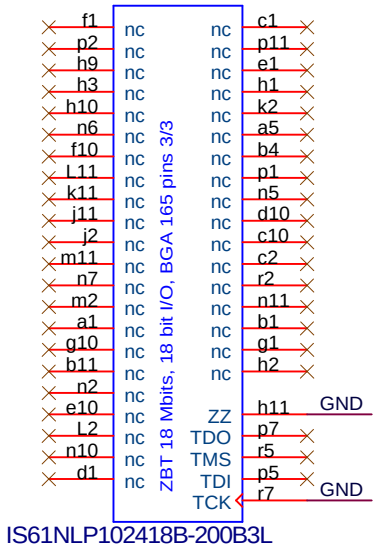
59 wires

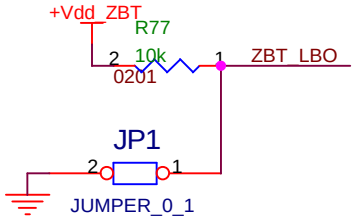
Byte Write Enable
ZBT_ben_[0:3]
ZBT_A[0:19]
ZBT_data[0:31]
ZBT_clk1
ZBT_clk2
ZBT_RW#
ZBT_adv_LD#

ZBT_OE# is not connected

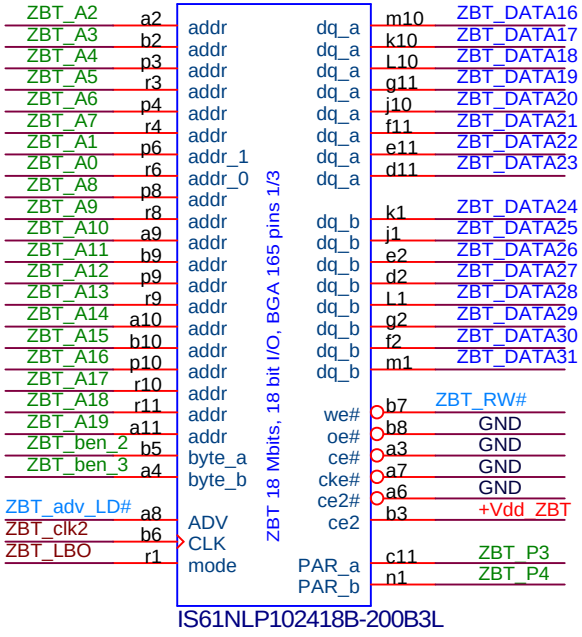
All IOs on this page are from the 3.3V banks.

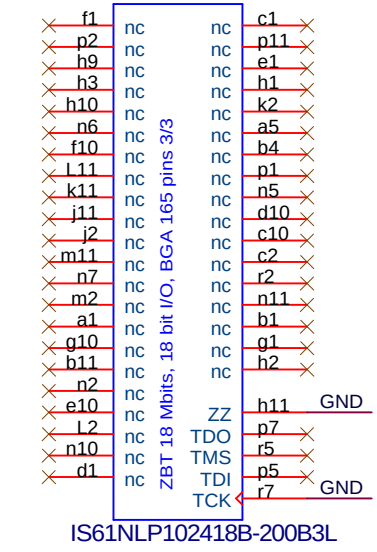




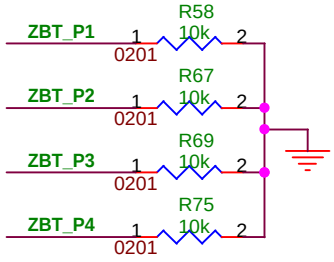


Linear Burst Order LBO is static. Must not change.
Choose HIGH or LOW according to the Data Sheet.





The parity bits are not used.



07/14/2018. PRELIMINARY prototype release for review. Not manufactured yet.

GND

Group 30

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 209
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
ZBT SRAM

Size	Document Number	Rev
A	A - RiskFive Artix Bone With ZBT Memory	0

Date: Friday, July 20, 2018 Sheet 22 of 29