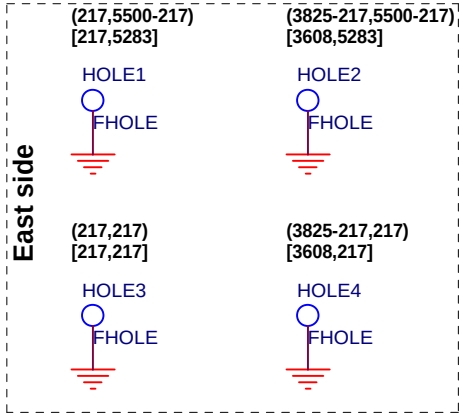
RiskZero LX9 Single Board Workstation Computer

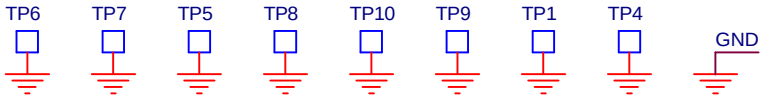
Rev	Description	Date	By
0.0	Initial release.	May/25/2020	WS
0.1	I2C expanders --> shift registers & 100k --> 10k on DIP page. Switchcraft --> CUI on FT2232HL page. Added pullups to PS/2.	Aug/22/2020	WS
0.1a	Added WiFi pin socket and WiFi documentation pages	Sept/26/2020	WS
B	---		WS
C	---		WS

Mounting holes



Sept/26/2020. PRELIMINARY prototype release for review. Not manufactured yet.

Note: Since this SBC was primarily designed to run the FPGA Oberon System by Niklaus Wirth, Juerg Gutknecht, and Paul Reed, the License for this board is the same as theirs. The original 2013 FPGA Oberon System is available from http://www.projectoberon.com/. Newer editions are referenced throughout the documentation.



SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title: Title page

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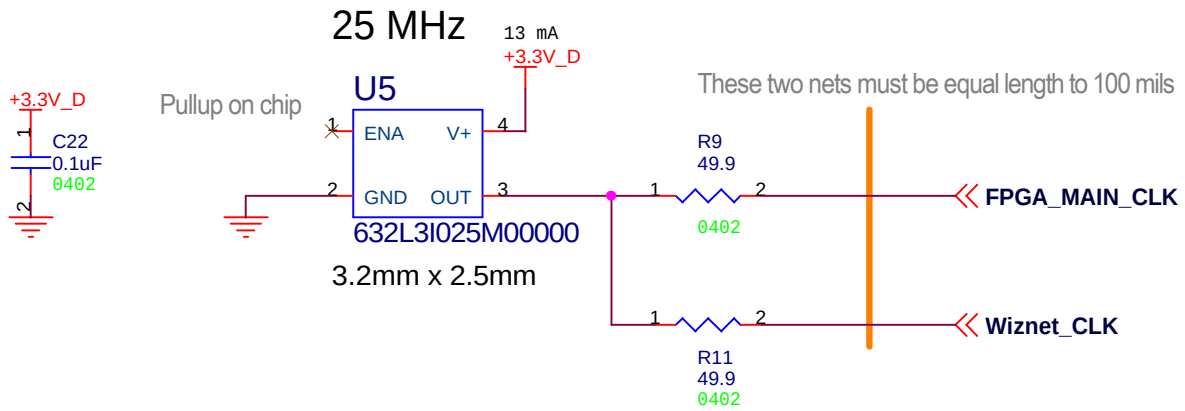
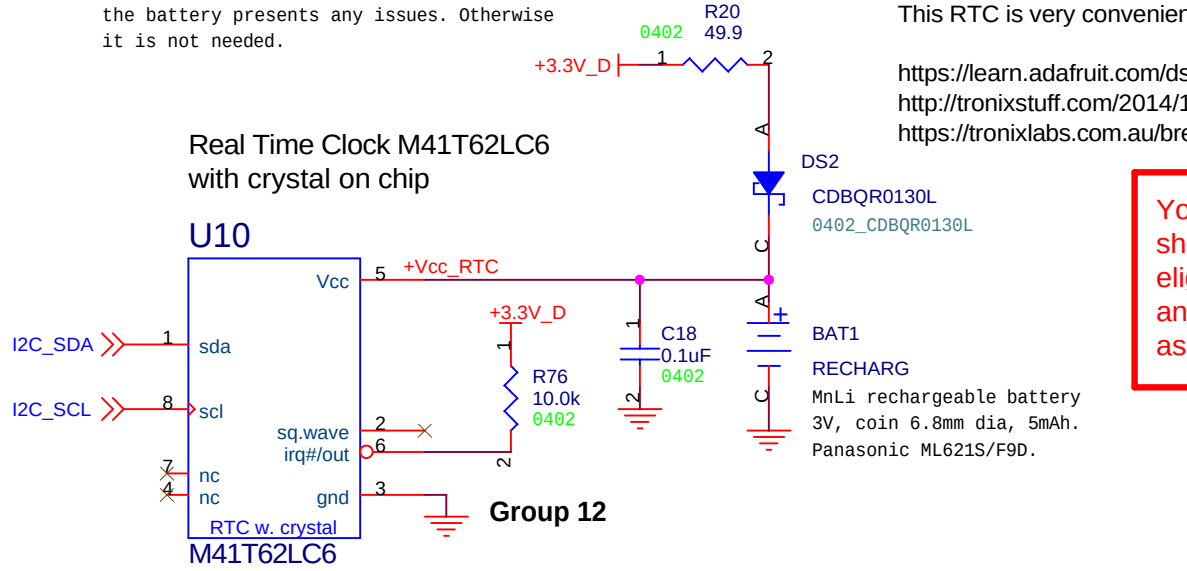
Clock driver 25 MHz CMOS 3.3V

This clock is driving the Ether chip and the FPGA. In order to avoid a fan-out buffer I am using two source-terminated nets of equal length.



I2C Real Time Clock with internal crystal

This resistor may need to get increased if the battery presents any issues. Otherwise it is not needed.



This RTC is very convenient and inexpensive. Code examples for Arduino can be found at the links below:

https://learn.adafruit.com/ds1307-real-time-clock-breakout-board-kit/understanding-the-code
http://tronixstuff.com/2014/12/01/tutorial-using-ds1307-and-ds3231-real-time-clock-modules-with-arduino/
https://tronixlabs.com.au/breakout-boards/real-time-clock/precision-ds3231-real-time-clock-module-australia/

You may not be able to assemble this battery overseas and get it shipped to the USA, because it is a "lithium battery" and thus not eligible for shipment. You may need to make it DNP in the BOM and add it later by hand. I do not know whether domestic assembly houses face the same restriction.

+3.3V_D GND

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Title: Main clock; also I2C RTC with battery backup

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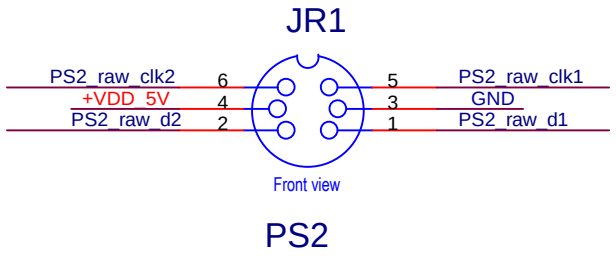
PS2 connectors

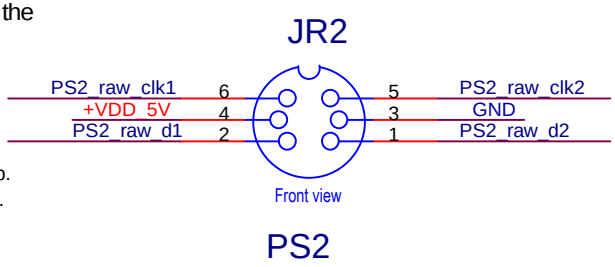
http://www.burtonsys.com/PS2_keyboard_and_mouse_mini-DIN-6_connector_pinouts.html
http://pinouts.ru/InputCables/Ps2KeyboardYThinkpad.shtml
http://pinouts.ru/Inputs/KeyboardPC6_pinout.shtml

Alternatively, this connector can be used as GPIO with 5V levels.

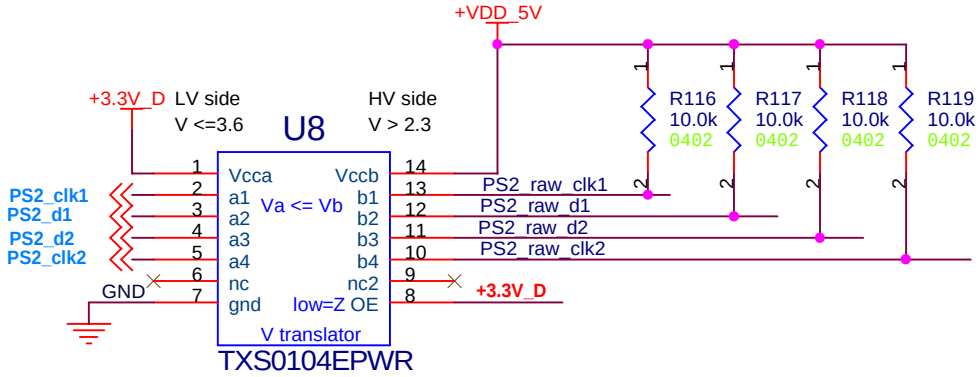
The wires are mirrored in these two connectors. Either one can be either the mouse or keyboard.
You must decide in firmware, which is which. Either can be used with a PS2 cable splitter.

https://en.wikipedia.org/wiki/PS%2F2_port
PS/2 protocol is bidirectional. We must use the bidirectional translator chip.





TXS0104 has OC outputs with 10k pullup on chip.
TXB0104 has push-pull outputs; it will NOT work.
OE active HIGH (!) is referenced to Vcca.



We have run into some problems with this chip in other designs. Pullups should help.

On this side it may be necessary to activate PULLUP in the FPGA.

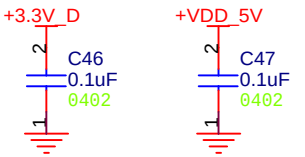
Bidirectional
voltage trans 4bit
TXS0104EPWR
$1.32/ea at
DigiKey

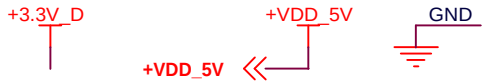
Mouse / keyboard Vcc = 5V
FPGA only tolerates 4V

http://pinouts.ru/InputCables/Ps2KeyboardYThinkpad.shtml

Con	signal	Keybrd	Mouse
1	dat1	----	1 (data)
2	dat2	1 (data)	----
3	gnd	3 (gnd)	3 (gnd)
4	Vcc	4 (Vcc)	4 (Vcc)
5	clk1	----	5 (clk)
6	clk2	5 (clk)	----

http://www.computer-engineering.org/ps2protocol/
Summary: Power Specifications
Vcc = +4.5V to +5.5V.
Max Current = 275 mA.





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Title
PS2 connectors

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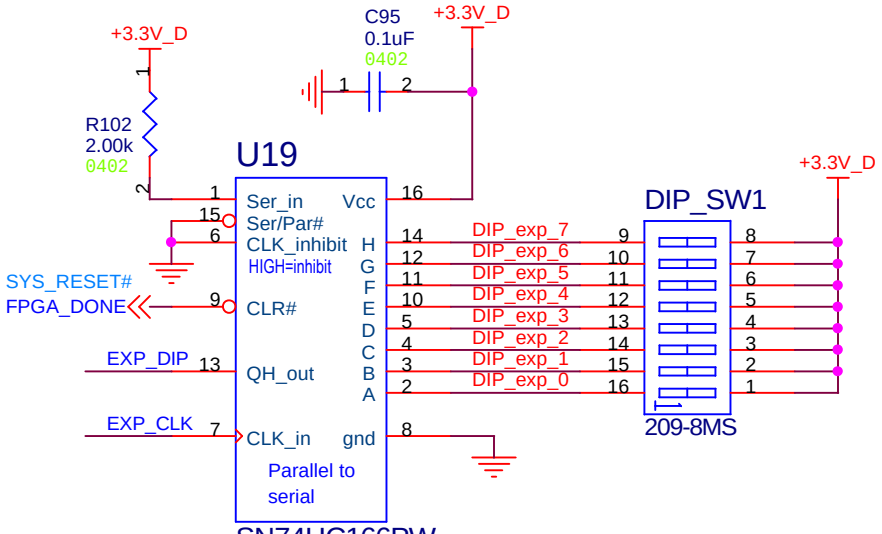
Shift register GPIO expanders

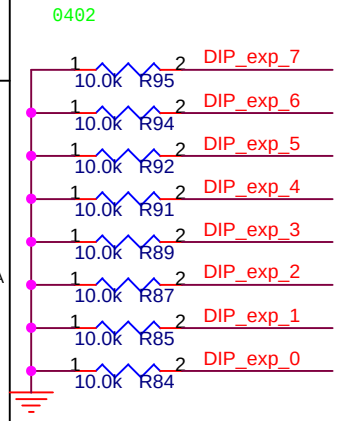
The FPGA does not have enough GPIO pins. We add pins via these chips.

Besides the "real" GPIO, this subsystem can demonstrate software background task scheduling. Put a task into the background loop which will turn LEDs on/off to create some sort of an eye pleasing pattern.

DIP switch input expander

Parallel to serial



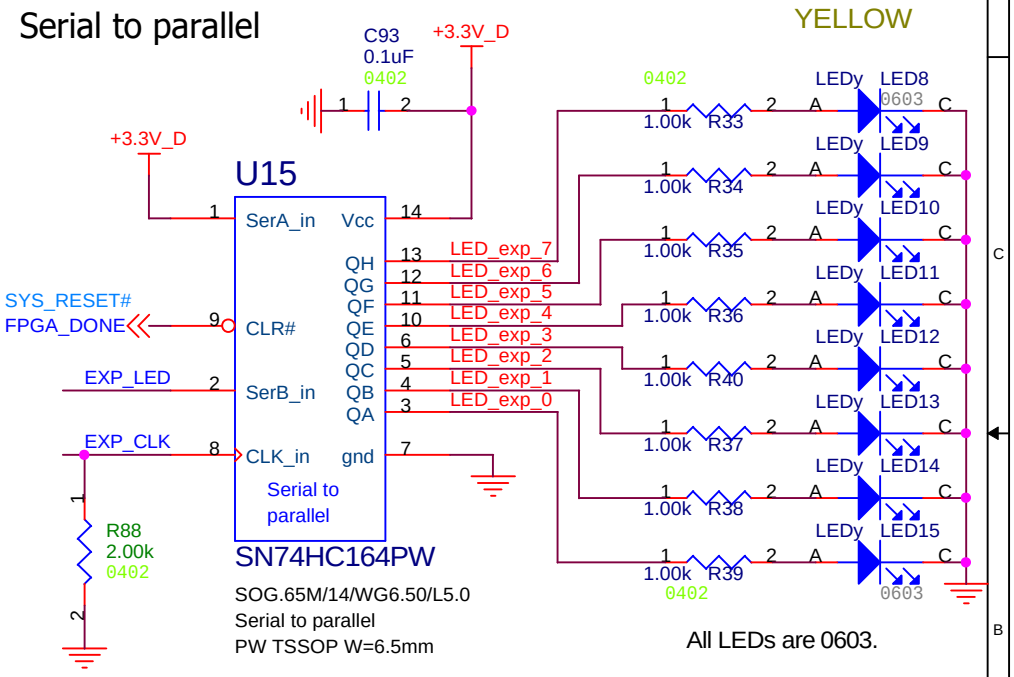


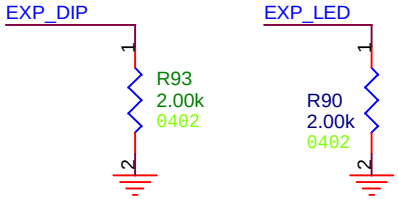
Expanders are on their own private expansion bus named EXP. These two expanders will provide fixed functions served with a firmware state machine. One is "in", the other is "out".

The reason is that RISC5 implements an "LED opcode" for a low level status display. I envision handling the LEDs transparently under the hood. I chose the shift registers rather than SPI or I2C because they are simpler.

LED display expander

Serial to parallel





DIP switch and LEDs

Separate pins from the main I2C

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Title: I2C expanders in (DIP switch) and out (LEDs)		(c) 2020 SkuTek Instrumentation. All rights reserved.
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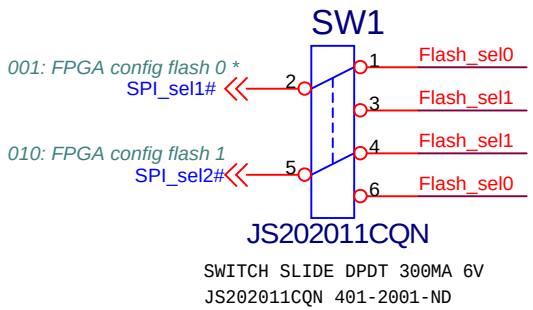
FPGA flash with dual boot switch

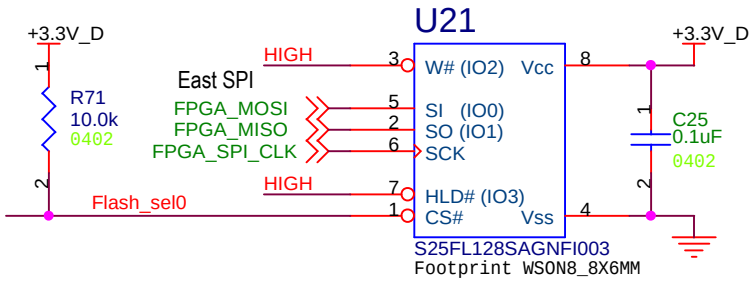
Avoid certain chips because Xilinx does not let program these from iMPACT or Vivado.
(You can program such chips with either fprog or s3prog, though.)

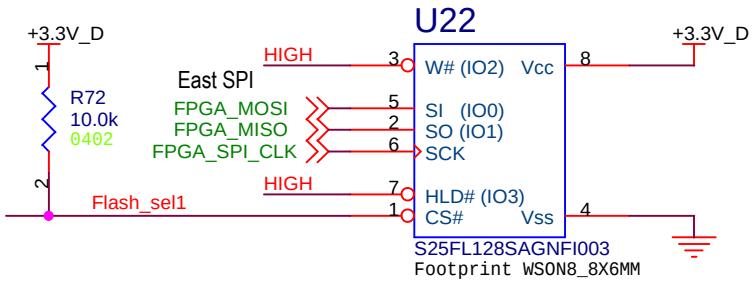
UG908 (v2020.1) June 3, 2020 Table 41 page 334
Supported flash devices
Spansion (now Cypress) s25flxxxs
Digikey on June/08/2020
S25FL128SAGNFI

2.7V..3.6V

UG380 Table 5-5, p.69
Bitstream file size (bits)
LX9 = 2,742,528 = 343kB
SPI modes 0 and 3.
Dual SPI uses IO0, IO1.
Quad SPI uses IO0..IO3.







XSPI

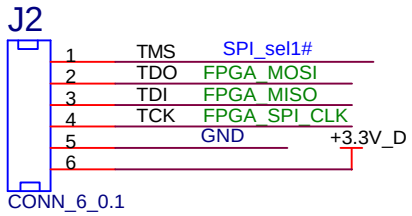
XSPI is an old programming utility from Xilinx. It worked with Parallel Cable III talking directly to the flash.

The FPGA SPI bus must be inactive while programming the config flash with XSPI pin header. This can be done with FPGA reset.

XSPI can configure the flash, while the FPGA is kept in reset.

Digilent Cable III pinout for XSPI utility.

Put FPGA in RESET while using the XSPI connector.



Flash chip notes

The flash is wired in the single and dual pin mode. Quad mode would require more FPGA pins than were available.

Since the bitstream file size is below 512 kB, half a meg flash would be sufficient. It is quite hard to find such small flashes anymore. A large flash (32 MB or more) can also be used for Oberon System disk beyond the first half a meg. Implementing the Oberon disk in a NOR flash may be attractive because the flash chip must always be present to boot the FPGA. A flash serving both roles would save both the board space and cost. Further notes are in the documentation pages.

Pullups are not needed because the SEL bits are driven push-pull. I am using the resistors because of my good habits.

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SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title: FPGA boot flash (two chips)

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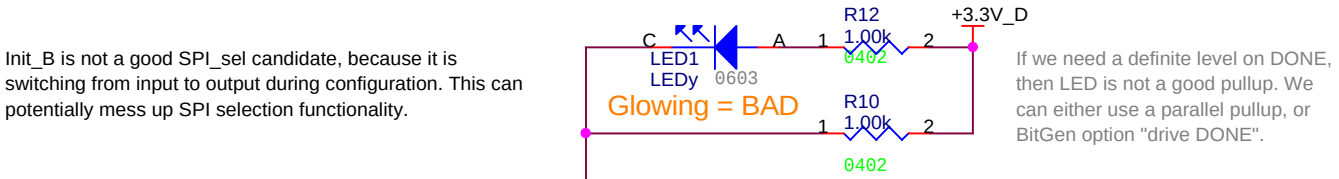
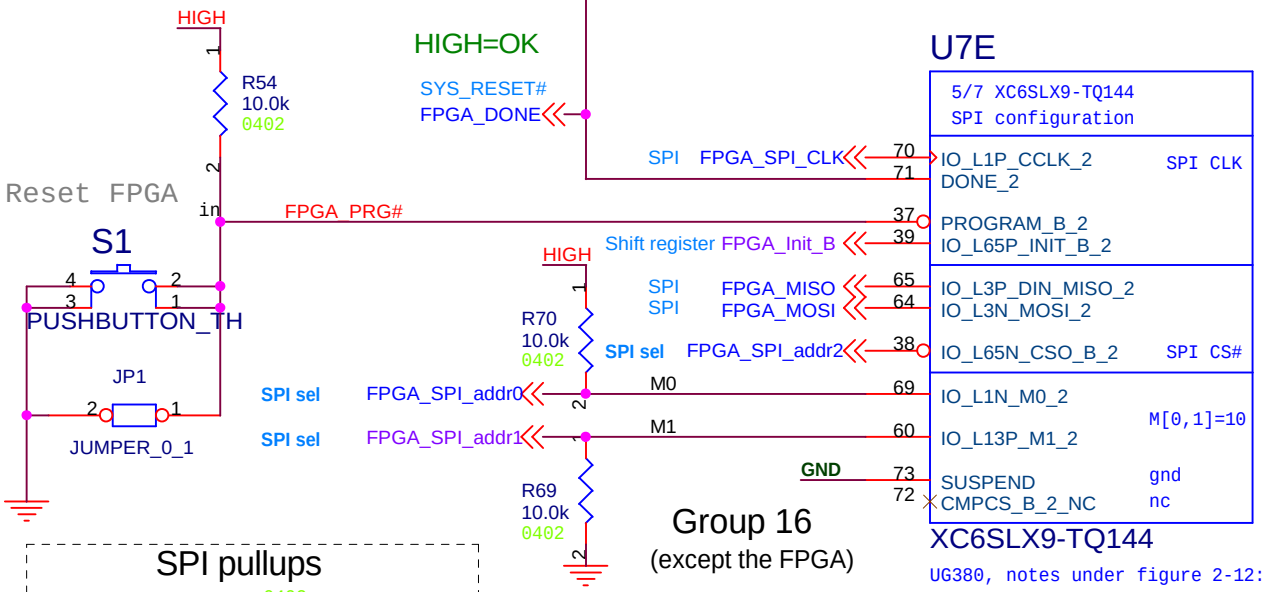
DS162.PDF, page 3: During configuration, if VCCO_2 is 1.8V, then VCCAUX must be 2.5V.

Init_B is not a good SPI_sel candidate, because it is switching from input to output during configuration. This can potentially mess up SPI selection functionality.

RED or YELLOW
DONE



If we need a definite level on DONE, then LED is not a good pullup. We can either use a parallel pullup, or BitGen option "drive DONE".



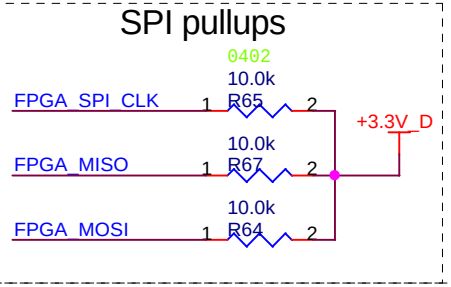
Group 16
(except the FPGA)

UG380, notes under figure 2-12: VCCO_2 supply must be the same voltage as VCC of the SPI device.

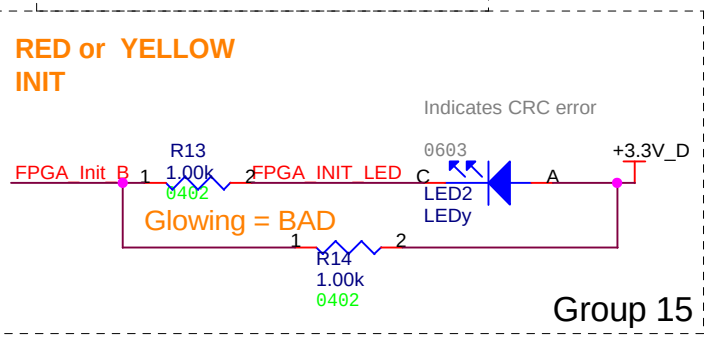
FPGA MOSI --> slave flash input (SI)
FPGA MISO --> slave flash output (SO)
UG380, Table 2-6

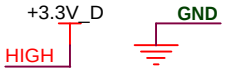
HSWAP_EN = LOW --> all non-config pins pulled up during config.

Pins become SPI after boot:
38: CSO_B = SPI_addr2
60: M1 = SPI_addr1
69: M0 = SPI_addr0
70: CCLK = SPI_CLK
64: SPI_MOSI
65: SPI_MISO
39: Init_B = shift register



On FPGA reset, ADDR[2,1,0] = [CSO_B, M1, M0] = (001) = Y1





FPGA Config Notes

HSWAP_EN = LOW --> enable weak pull-ups PRIOR TO AND DURING CONFIGURATION on all non-configured pins, including M-pins. The pullups are turned OFF after configuration and replaced with PULLDOWNS. (SelectIO User Guide UG381 v. 1.2 p.43).

BitGen option UnusedPins will allow to retain PULLUPS on all unconfigured pins.

```
HSWAP_EN has internal pullup.
HSWAP_EN    input
CCLK        input/output
PROG_B      input
DONE        input or open drain
Use "DRIVEDONE" option in FPGA bitstream to
make it push-pull.
```

FPGA SPI Config Notes

XSPIcan reprogram FPGA boot flash. The same FPGA boot flash is accessed by XSPI, FTDI, or the FPGA, using the same MOSI / MISO pair. The FPGA must be put into reset before the external entity is accessing flash.

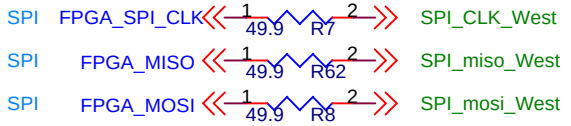
Pullups on MISO / MOSI / CLK are quite strong to make sure they overcome internal FPGA PU/PD. Pullup on MISO is necessary for the SD card init.

There is no point in adding pullups to the SPI CS# lines because these are driven by the push-pull 3-to-8 decoder chip.

```
PRGM   -   initiate FPGA prgm
DONE   -   verify FPGA prgm
InitB  -   verify FPGA prgm
```

After config the Init_B can be the I/O pin

West side of the board



SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title: FPGA configuration interface

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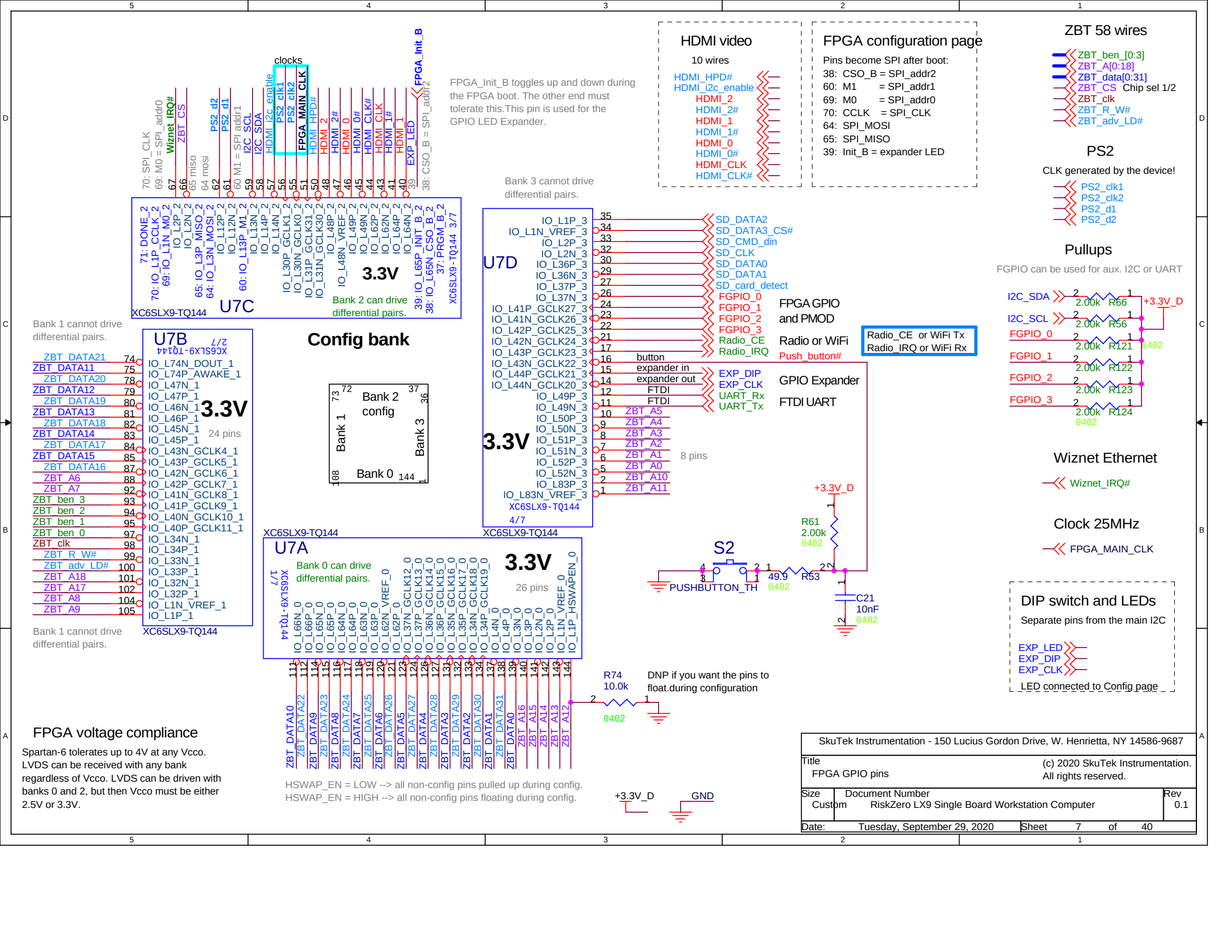
clocks
FPGA_Init_B toggles up and down during the FPGA boot. The other end must tolerate this.This pin is used for the GPIO LED Expander.
HDMI video
10 wires
HDMI_HPD#
HDMI_i2c_enable
HDMI_2
HDMI_2#
HDMI_1
HDMI_1#
HDMI_0
HDMI_0#
HDMI_CLK
HDMI_CLK#
FPGA configuration page
Pins become SPI after boot:
38: CSO_B = SPI_addr2
60: M1 = SPI_addr1
69: M0 = SPI_addr0
70: CCLK = SPI_CLK
64: SPI_MOSI
65: SPI_MISO
39: Init_B = expander LED
ZBT 58 wires
ZBT_ben_[0:3]
ZBT_A[0:18]
ZBT_data[0:31]
ZBT_CS Chip sel 1/2
ZBT_clk
ZBT_R_W#
ZBT_adv_LD#
PS2
CLK generated by the device!
PS2_clk1
PS2_clk2
PS2_d1
PS2_d2
Pullups
FGPIO can be used for aux. I2C or UART
Bank 3 cannot drive differential pairs.
U7D
3.3V
FPGA GPIO and PMOD
Radio or WiFi
Radio_CE or WiFi Tx
Radio_IRQ or WiFi Rx
Push_button#
GPIO Expander
FTDI UART
8 pins
Bank 1 cannot drive differential pairs.
U7B
24 pins
Config bank
Bank 2 config
Bank 1
Bank 3
Bank 0
Bank 2 can drive differential pairs.
U7C
XC6SLX9-TQ144
U7A
Bank 0 can drive differential pairs.
26 pins
S2
PUSHBUTTON_TH
R61 2.00k 0402
R53 49.9 0402
C21 10nF 0402
R74 10.0k 0402
DNP if you want the pins to float.during configuration
Wiznet Ethernet
Wiznet_IRQ#
Clock 25MHz
FPGA_MAIN_CLK
DIP switch and LEDs
Separate pins from the main I2C
EXP_LED
EXP_DIP
EXP_CLK
LED connected to Config page
FPGA voltage compliance
Spartan-6 tolerates up to 4V at any Vcco. LVDS can be received with any bank regardless of Vcco. LVDS can be driven with banks 0 and 2, but then Vcco must be either 2.5V or 3.3V.
HSWAP_EN = LOW --> all non-config pins pulled up during config.
HSWAP_EN = HIGH --> all non-config pins floating during config.
+3.3V_D
GND
SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687
Title
FPGA GPIO pins
(c) 2020 SkuTek Instrumentation. All rights reserved.
Size
Custom
Document Number
RiskZero LX9 Single Board Workstation Computer
Rev
0.1
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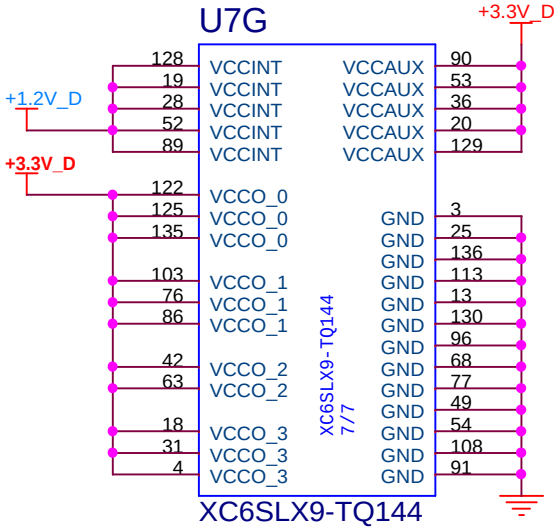
FPGA power and JTAG

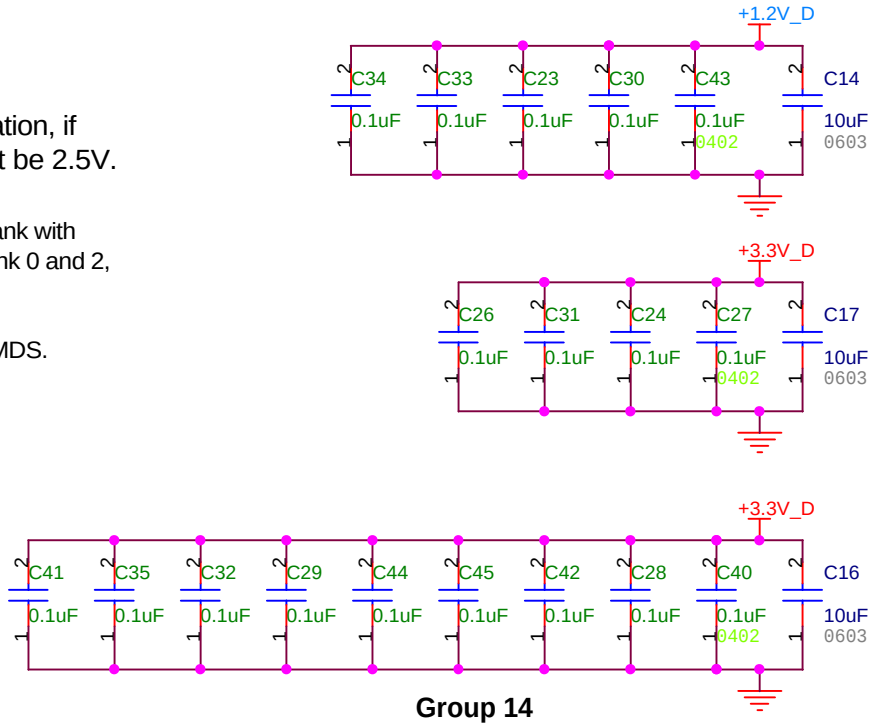


DS162.PDF, page 3: During configuration, if VCCO_2 is 1.8V, then VCCAUX must be 2.5V.

Differential signals can be received in any bank with any Vcco. Differential can be output from Bank 0 and 2, if they are powered with 2.5V or 3.3V.

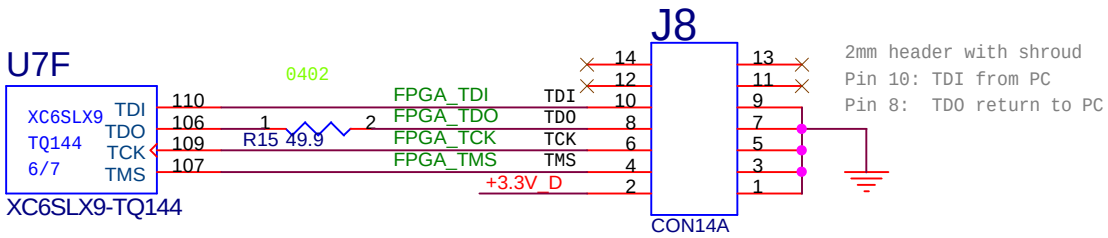
In this design we are outputting differential TMDS.

Config

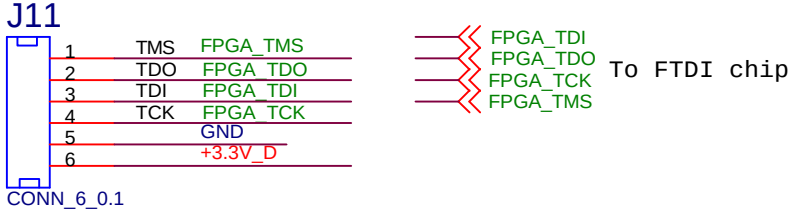


Group 14

Xilinx Parallel Cable IV



Xilinx Parallel Cable III



Group 0

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687		
Title: FPGA power pins and JTAG pins	(c) 2020 SkuTek Instrumentation. All rights reserved.	
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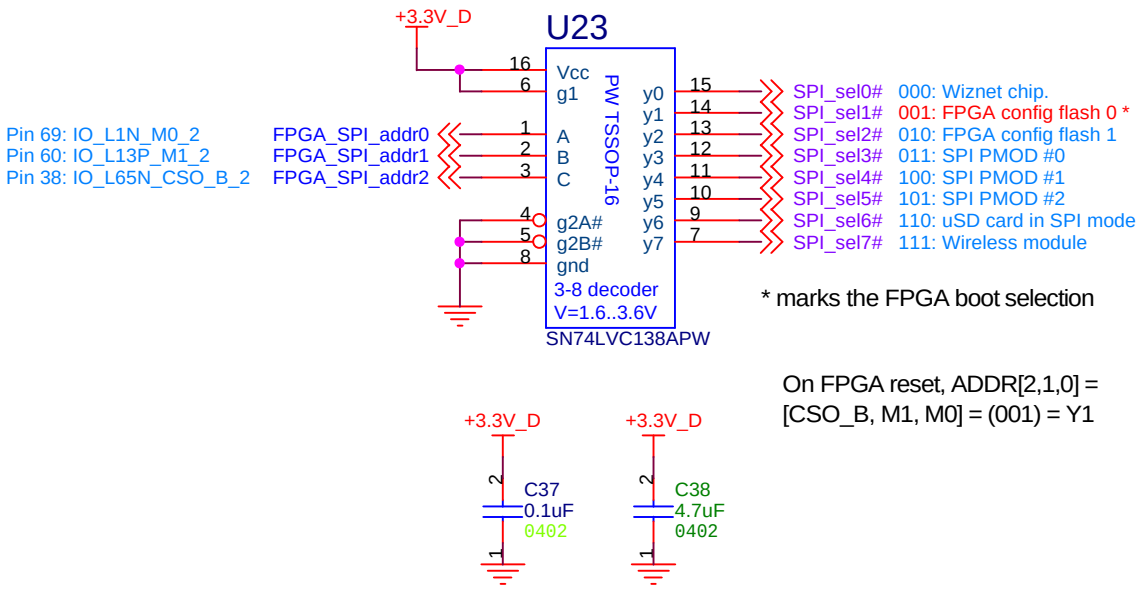
SPI device selection

There is one SPI bus serving several devices.

SPI address decoder



* marks the FPGA boot selection

On FPGA reset, ADDR[2,1,0] = [CSO_B, M1, M0] = (001) = Y1

SPI addressing notes

This chip uses push-pull active drive. No point in adding pullups to the SPI CS# lines because these are driven by the push-pull chip.

After resetting the FPGA the address bits will be (CS#, M1, M0) = "001" because M0 has a pullup, M1 a pull down, and CS# is driven LOW. Hence, the FPGA config flash must be connected to Y1 = SPI_sel1. After the FPGA boot, the address bits must be managed by the embedded firmware and software running inside the FPGA.

Note that flash 0 and flash 1 can be swapped with a slide switch. This will allow to swap two boot images. It is also possible to use one flash for boot, and the other as a disk. Finally, since both flash chips will be quite large (32 MB or so), they both can be used as solid state disks beyond the first 512 kB needed for booting the FPGA.

The full size SD card is using a dedicated bus. It does not participate in the SPI addressing protocol. It means that the full size SD card can use its own SPI controller, perhaps different from the "device SPI" implemented here.

The full size SD can use the QSPI protocol because all the SD pins are connected to the FPGA. The micro SD can only use the single SPI because only the SPI pins of the uSD are connected. This is why the uSD is here, while the full size SD is not.

It means that the uSD card is ready for the Oberon System. The full size SD can be used with single SPI as well, though it is tempting to enhance its performance with full QSPI.

SN74LVC138APW 3to8 decoder
SOG.65M/16/WG8.20/L6.35
All the following are the same:
SN74LVC138APWR
SN74LVC138APWT
SN74LVC138APWRG4

Group 27

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title: SPI subsystems address generator

Size	Document Number	Rev
A	RiskZero LX9 Single Board Workstation Computer	0.1

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USB Serial and JTAG

FT2232HL LQFP_64 USB_Serial

https://gist.github.com/rikka0w0/24b58b54473227502fa0334bbe75c3c1

To Power Entry page

Connecting RESET# to FPGA_DONE would create a dead latch.

P2 — USB_Mini_5pin

U24 — 93LC46BT-I/OT
EEPROM Memory IC 1Kb (64 x 16)
SPI 2MHz SOT-23-6

U18 — ASV-12.000MHZ-EJ-T
Footprint FOX\F4100
7mm x 5mm

U17F — FT2232HL

U17A — FT2232HL

U17C — FT2232HL

U17D — FT2232HL

U17E — FT2232HL

Header for FTDI cable, in case FT2232 does not work

Pullup on chip

PWR source select

Current sensing

BDBUS is all NC and thus not shown

RTS connected to CTS

UART can be used either for the debugging with the FTDI, or for communication with peripherals. Install the jumpers for the former.

Resistors insulate the JTAG connector from FTDI drivers if the USB is trying to drive the pins while the JTAG cable is plugged in.

Suspend detection may be in conflict with pin programming. See Data Sheet page 71, which however seems to be in error. They say "BDBUS7", while in fact it is BCBUS7.

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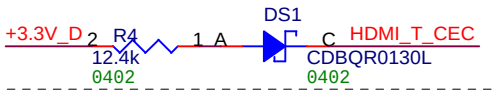
Title: FTDI USB serial and JTAG	(c) 2020 SkuTek Instrumentation. All rights reserved.
Size: A	Document Number: RiskZero LX9 Single Board Workstation Computer — Rev: 0.1
Date: Tuesday, September 29, 2020	Sheet 10 of 40

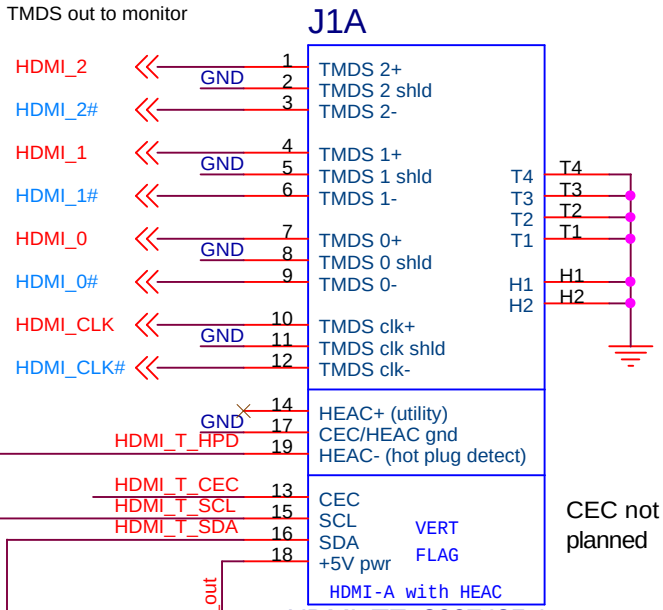
HDMI driver for video output: 10 pins (w/o CEC; w/o I2C)

Tech info about CEC: https://elinux.org/CEC_(Consumer_Electronics_Control)_over_HDMI

CEC is pulled up Via Schottky. Schottky and 27k were used in BBB. Not sure why the Schottky is needed. Here I used 12k.



TMDS out to monitor

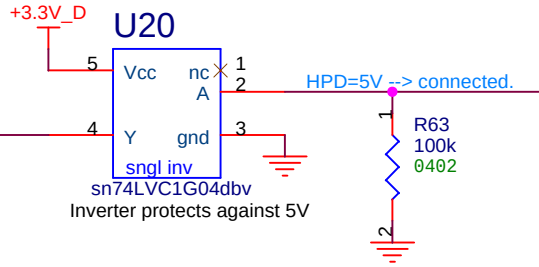


HDMI_TE_2007435-1

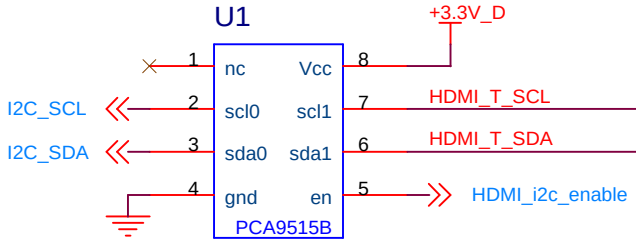
Footprint HDMI_TE_2007435-1

CEC not planned

Single inverter SOT23-5
Active push-pull



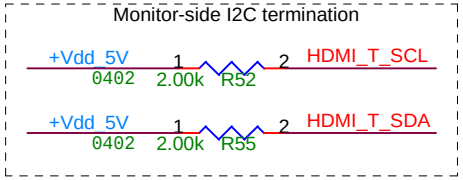
sn74LVC1G04dbv
Inverter protects against 5V

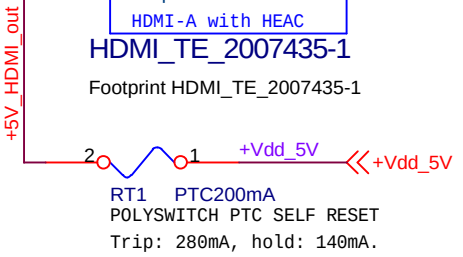


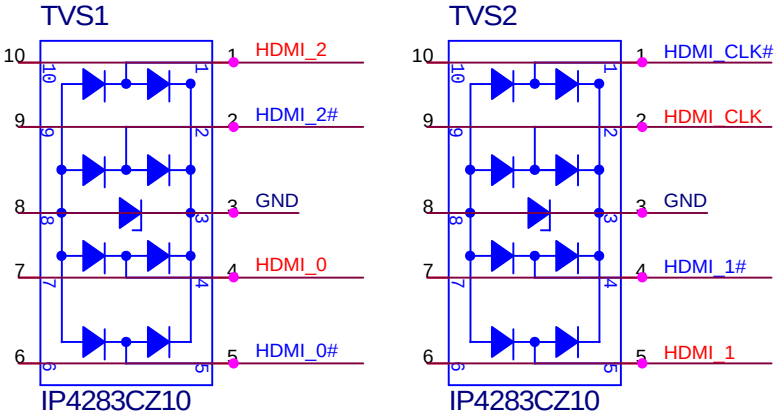
PCA9515BDGKR

I2C repeater with translation
SOG.65M/8/WG4.00/L3.00

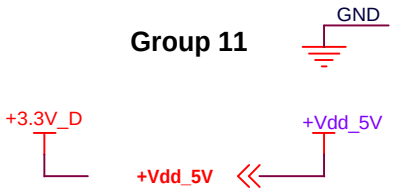
Board-side I2C termination is provided elsewhere







Group 11



HDMI Notes

LCD to HDMI converter is available from Open Cores. It is a generic IP that does not necesitate any setup. Default timing setups are provided for different display resolutions of the LCD IP.

https://opencores.org/projects/lcd_to_hdmi_output_ip

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Title: HDMI video connector

Size: A | Document Number: RiskZero LX9 Single Board Workstation Computer | Rev: 0.1

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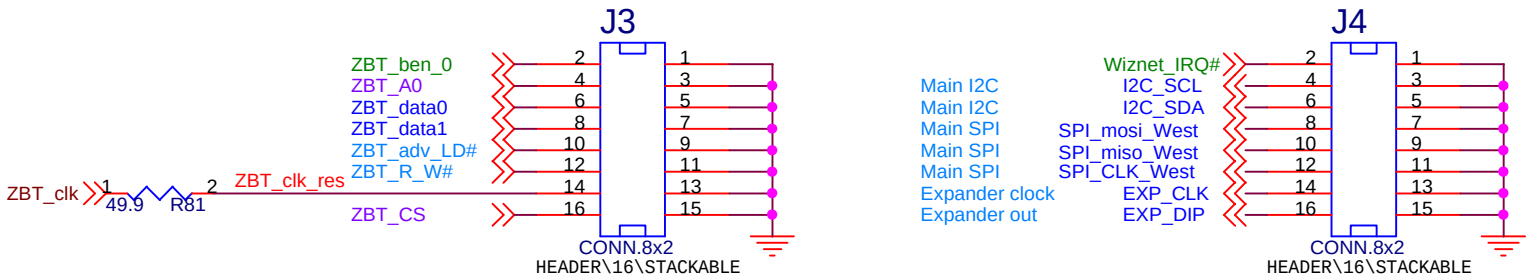
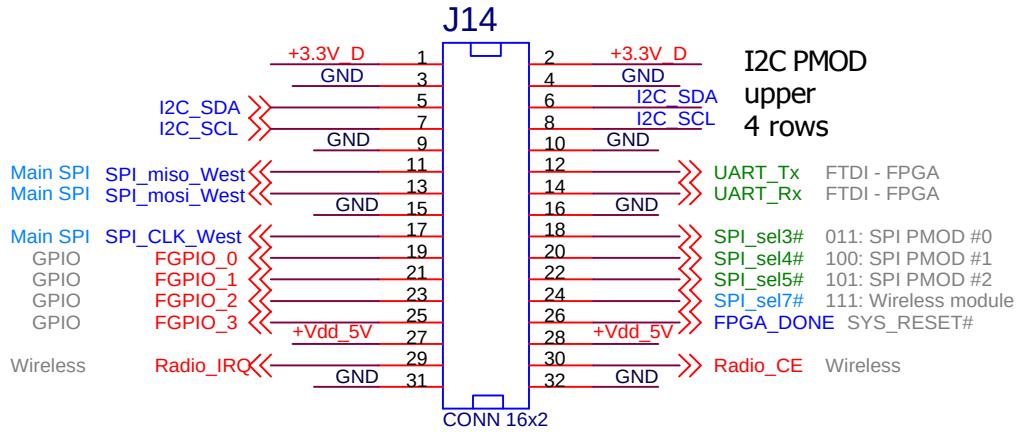
Pin headers: Logic Analyzer and Peripheral Expansion

The headers are intended for the mixed-mode Tektronix oscilloscope with 16 digital capture channels (two 8-channel cables).

The third header can be used to connect peripherals. The pins are shared with PMOD and wireless due to shortage of pins.



This header can be used to connect peripherals or to develop an expansion card using cheap pre-perf boards.



I2C PMOD upper 4 rows

I2C PMOD connector

Strictly speaking, Digilent says it is not PMOD. They define it nevertheless on Page 4 and 6 of their PMOD definition document.

Expansion connector

The GPIO or SPI_sel pins can be used to connect scope probes. If they are used for an expansion board, then the PMOD and wireless should not be used.

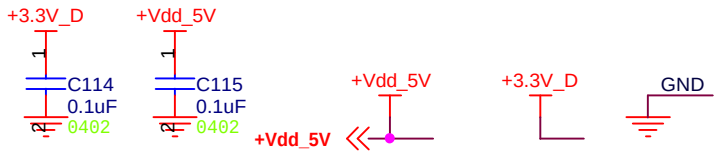
UART

This UART is connected to the FTDI and FPGA. It is discouraged to use it for the expansion UART, because then you cannot use it for communication with the PC host. If you need an UART on the expansion board then use GPIO pins to implement another dedicated UART,

Part Numbers

```
CONN HEADER VERT 34POS 2.54MM
34 pos TSW-117-07-G-D Samtec
CONN HEADER VERT 32POS 2.54MM
32 pos TSW-116-07-G-D Samtec
CONN RCPT 32POS 0.1 TIN PCB
32 pos SSW-116-01-T-D Samtec
CONN RCPT 32POS 0.1 GOLD PCB
32 pos SSW-116-02-G-D Samtec

24 positions 6-146256-2
16 positions 77313-818-16LF
```



SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title: Diagnostic pin headers

Size	Document Number	Rev
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Digilent Pmod-Compatible connectors with SPI and FPGA GPIO

Digilent Pmod™ Interface Specification 1.2.0; Revised October 5, 2017

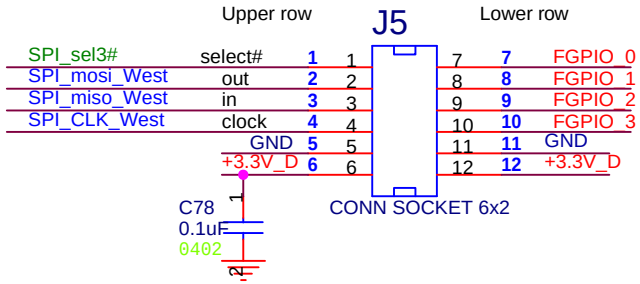
Upper row of the Pmod Interface Type 2 (SPI) is the same as the Digilent JTAG Cable III pinout. The lower row is not well specified in the Digilent document. Several of their PMODs utilize GPIOs on the lower row. For example, the lower row implements interrupt pins in several PMODs.

Note non-standard pin numbering (in bold) of 12-pin headers.

Part number: PPPC062LJBN-RC
Sullins; right angle female

SPI PMOD 0

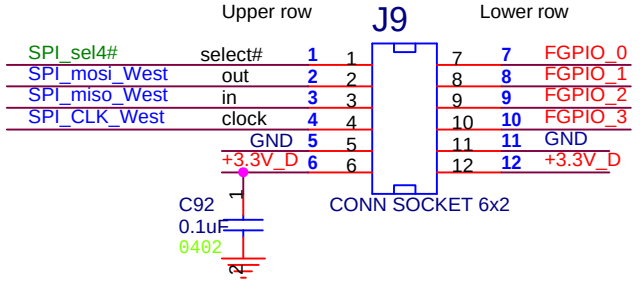
SPI SEL 3



Inside of the board

SPI PMOD 1

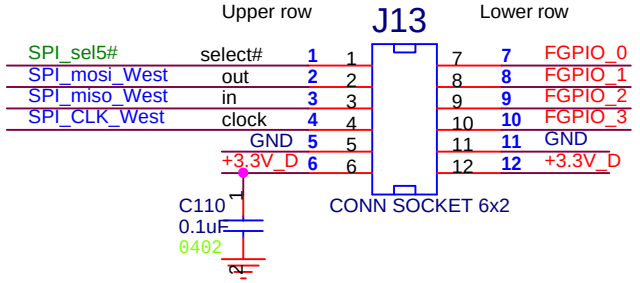
SPI SEL 4



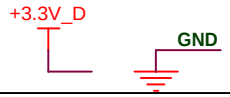
Inside of the board

SPI PMOD 2

SPI SEL 5



Board Edge - PMOD boards are here



SPI PMOD Notes

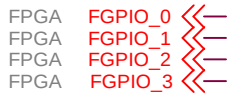
These connectors are Digilent Pmod Compatible, as specified in Pmod licensing requirement.

These are "slow PMOD" connectors for slow serial ADC or DAC chips. You can build a closed loop control instrument, temperature monitor, stepping motor controller, etc. Digilent offers many valuable PMOD modules which can be used for many projects.

The PMODs share all signals except for chip select. It means that they have to be operated sequentially by the software. (E.g., read PMOD 0, then read PMOD 1, etc.) It is a good match to a single core, single process multitasking Oberon System.

The SPI signals are shared with the FPGA boot flash, Wiznet W5500, and the microSD card. Note that the full size SD card is not sharing this bus.

West SPI is driven via 50 ohm serial termination



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Title: Three PMOD connectors; and one I2C pseudo-PMOD

Size	Document Number	Rev
A	RiskZero LX9 Single Board Workstation Computer	0.1

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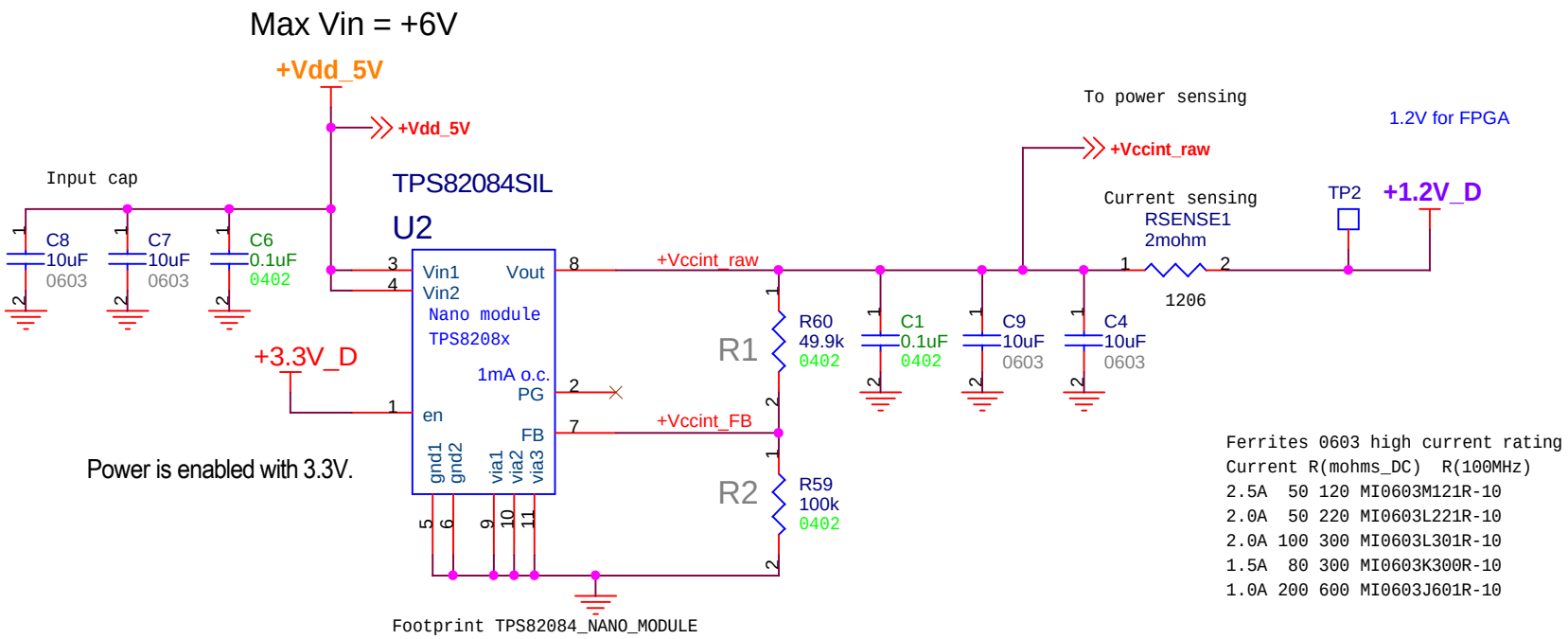
1.2V for FPGA Vccint.



Ferrites 0603 high current rating

Current	R(mohms_DC)	R(100MHz)	
2.5A	50	120	MI0603M121R-10
2.0A	50	220	MI0603L221R-10
2.0A	100	300	MI0603L301R-10
1.5A	80	300	MI0603K300R-10
1.0A	200	600	MI0603J601R-10

TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
Vout = 1.00V --> R1 = 24.9 k
Vout = 1.20V --> R1 = 49.9 k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.80V --> R1 = 124 k
Vout = 2.50V --> R1 = 215 k
Vout = 3.30V --> R1 = 309 k
Assuming R2 = 100k
```

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
TPS82084SIL    $3.11   2 A *
TPS82085SIL    $4.05   3 A *
```

GND

Group 20

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title: DC/DC for the FPGA core (Vccint)

Size: A | Document Number: RiskZero LX9 Single Board Workstation Computer | Rev: 0.1

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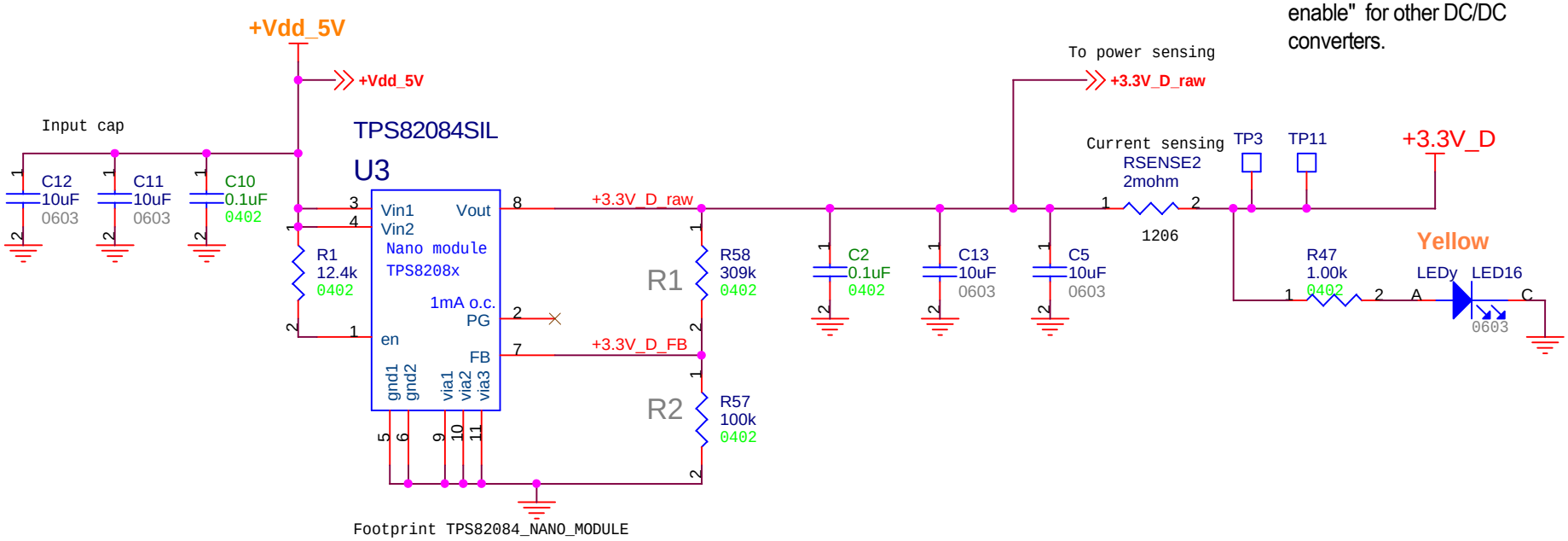
3.3V for all on-board circuits.

```
Ferrites 0603 high current rating
Current R(mohms_DC)  R(100MHz)
2.5A  50 120 MI0603M121R-10
2.0A  50 220 MI0603L221R-10
2.0A 100 300 MI0603L301R-10
1.5A  80 300 MI0603K300R-10
1.0A 200 600 MI0603J601R-10
```

+3.3V_D serves as "power enable" for other DC/DC converters.

Max Vin = +6V



TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
Vout = 1.00V --> R1 = 24.9 k
Vout = 1.20V --> R1 = 49.9 k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.80V --> R1 = 124 k
Vout = 2.50V --> R1 = 215 k
Vout = 3.30V --> R1 = 309 k
Assuming R2 = 100k
```

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
TPS82084SIL    $3.11   2 A *
TPS82085SIL    $4.05   3 A *
```

GND

Group 18

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title: FTDI USB serial and JTAG

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A	RiskZero LX9 Single Board Workstation Computer	0.1

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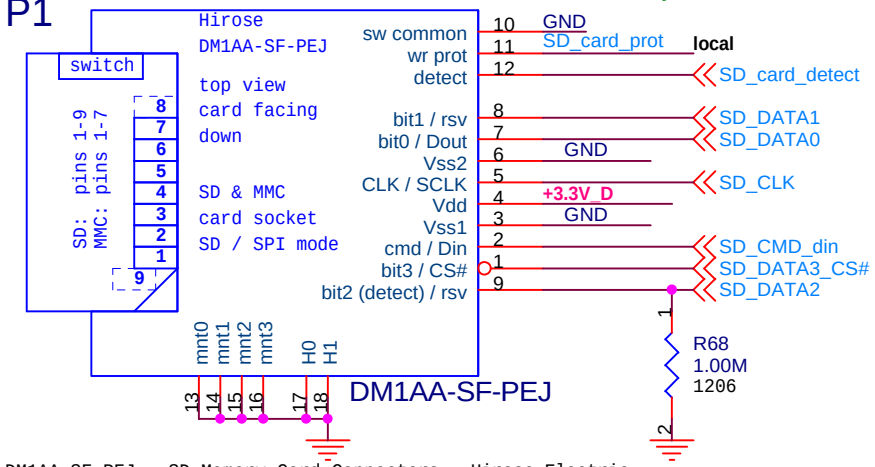
SD / MMC full size card socket

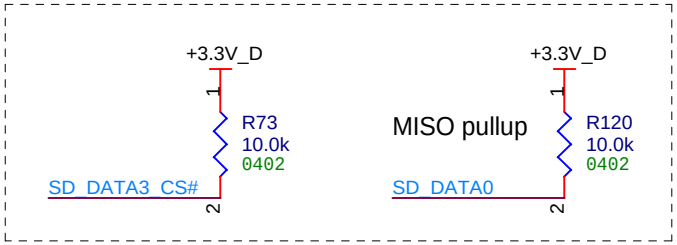
http://elm-chan.org/docs/mmc/mmc_e.html
Explained SPI operation of SD card

Still available on
May/15/2020

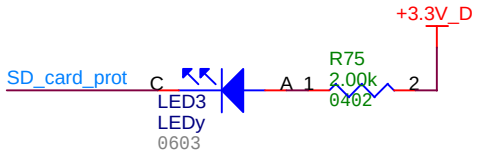
SD card draws up to 100mA

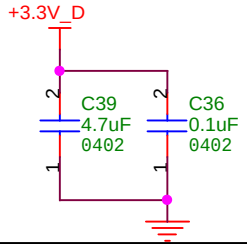


DM1AA-SF-PEJ - SD Memory Card Connectors - Hirose Electric
DigiKey HR845CT-ND $3.80



A visual indication of the SD card protection switch.





Notes

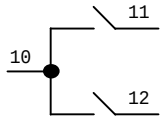
SD card is connected to the FPGA with its own wires, not using the board-wide SPI bus. Either the SPI or the full QSPI can be used for communication with the card.

Support for SD 4-bit mode, compliant with SD Host Controller Spec version 2.0, is provided by Open Cores. This FPGA may be too small for the implementation. A larger FPGA may be needed in the future.

http://opencores.org/project,sdcard_mass_storage_controller
http://opencores.org/project,sd_card_controller

If QSPI is not used then use SPI mode 0. Pullup on MISO is necessary for card initialization. Note that this MISO is not the same as the FPGA "official MISO" from the configuration pins.

There are two switches, one for the card insertion and one for write protection. MMC card does not provide the latter switch. I did not connect the write protect to the FPGA. It is only indicated with an LED. Software can detect the card presence via the card detect switch. It can be routed to an interrupt. This will be valuable if the SW is running off the micro SD, using the full SD for data storage.



Bit2 (detect) has on-card pullup
50k used to detect the SD card. A
large pulldown is needed here.

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Title SD card full size and QSPI interface		(c) 2020 SkuTek Instrumentation. All rights reserved.
Size A	Document Number RiskZero LX9 Single Board Workstation Computer	Rev 0.1
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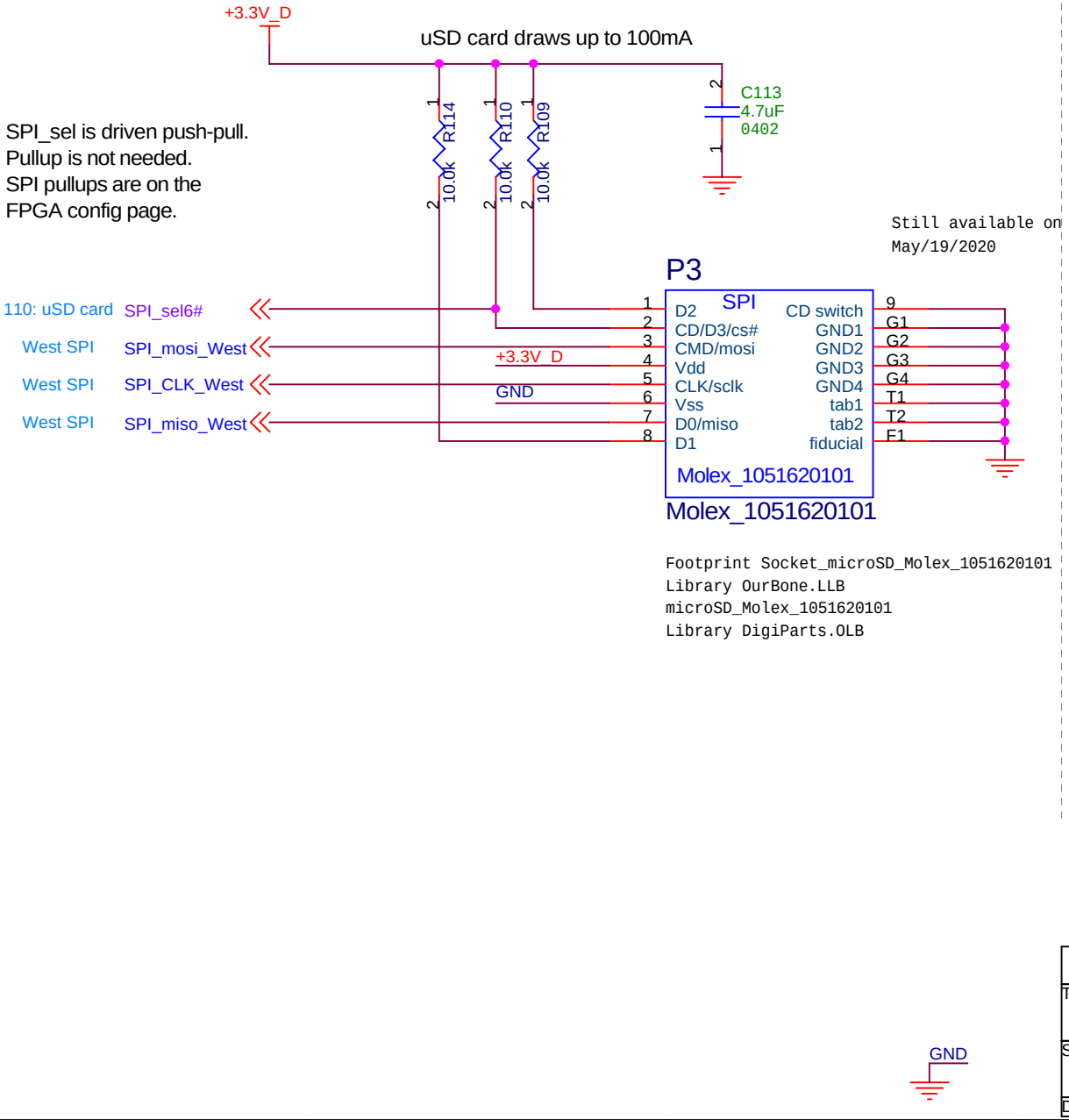
uSD socket

http://elm-chan.org/docs/mmc/mmc_e.html
Explained SPI operation of SD card



uSD card notes

The uSD card can only be operated in SPI mode. It is the only mode currently handled under the FPGA Oberon System (May/2020). This mode does not require a license. On the other hand, the quad SD card core blocks are available from the internet. The other SD card is wired in the quad mode (the full size socket).

This card can be used as the Oberon System main disk. The other card can be used as a data storage device. Development and testing of alternative file system fill be easier when the main system disk (this card) is not affected by the development of the other card.

The roles of the two cards can be reversed.

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title
SD card micro size with SPI interface

Size A | Document Number RiskZero LX9 Single Board Workstation Computer | Rev 0.1

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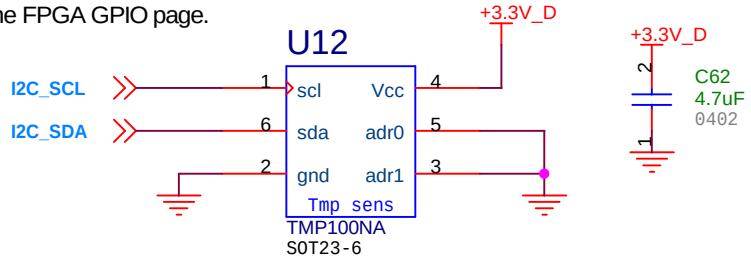
I2C Temp sensor

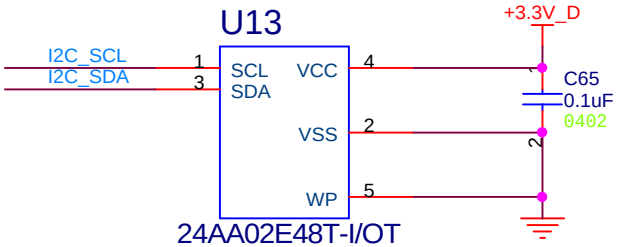
TMP100NA 12-bit temp sensor
SOT-23 (6 pads)

Pullups are on the FPGA GPIO page.



ADD = (0,0) => 1001000
Decimal = 72

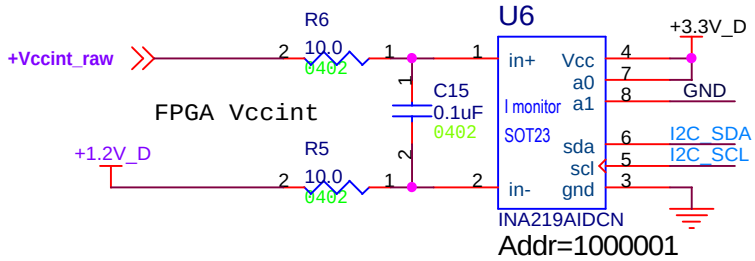
Ethernet MAC EEPROM

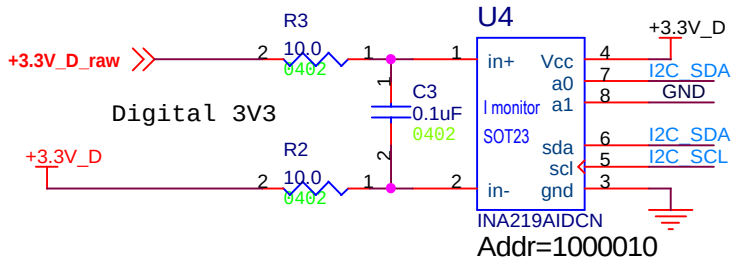


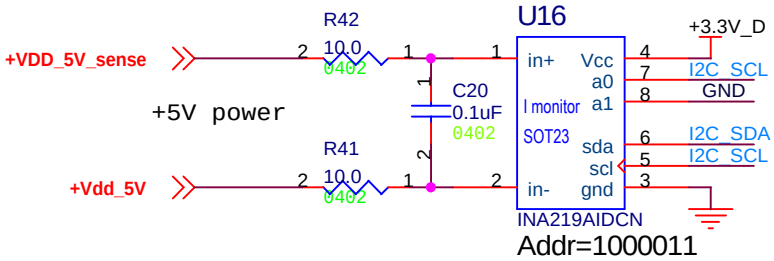
WP pin is n.c. in this part

MAC ID EPPROM on I2C0
Plastic SOT-23, 5-lead
Address = 1010 000

Voltage and current monitors







GND

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title
T sensor, MAC EEPROM, and PWR monitors

Size	Document Number	Rev
A	RiskZero LX9 Single Board Workstation Computer	0.1

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SPI connector for wireless or other uses

The socket pinout is compatible with the NRF24L01 wireless module used in 2013 FPGA Oberon.
Remember: This is just a socket! Another SPI application is possible as well.

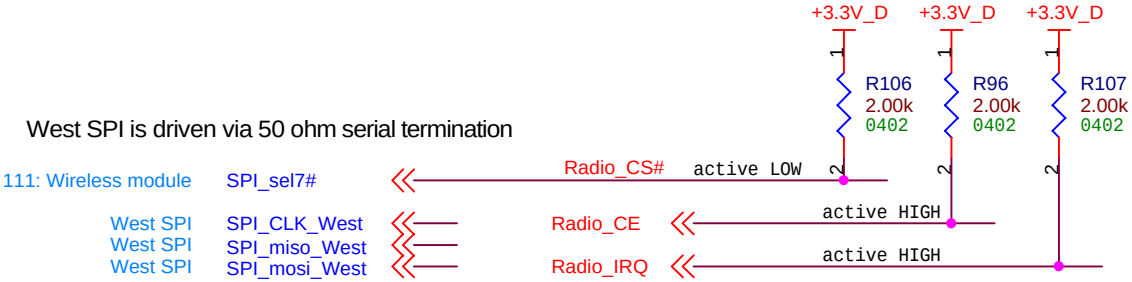
Search Amazon for "nrf24l01 transceiver module" and you will find plenety of these. You can develop your own such module with ESP32 or similar chips. You can also run flying wires from this connector to a a module with incompatible pinout. Examples from Amazon:

How to purchase the wireless module

1) Aideepen 2PCS NRF24L01 Wireless Transceiver Module+2.4GHz Antenna for Arduino
2) DEVMO 2PCS Compatible with Arduino NRF24L01+ 2.4GHz Wireless Transceiver
3) MakerFocus 2pcs NRF24L01+PA+LNA Wireless Transceiver RF Transceiver Module

http://www.nordicsemi.com/eng/Products/2.4GHz-RF/nRF24L01P
Nordic Semiconductor
nRF24L01P_Product_Specification_1_0.pdf; Page 50.
See also: http://randomnerdtutorials.com/nrf24l01-2-4ghz-rf-transceiver-module-with-arduino/
https://gadgetperfect.wordpress.com/nrf24l001-rf-module2-4ghzinterfacing/

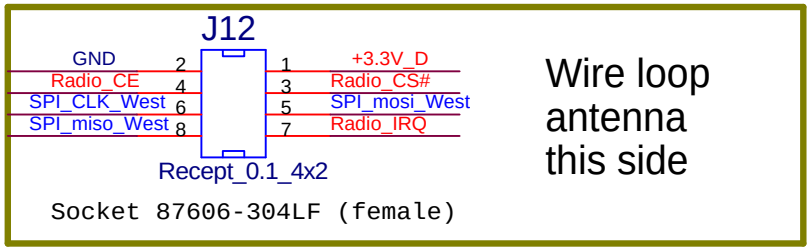
West SPI is driven via 50 ohm serial termination

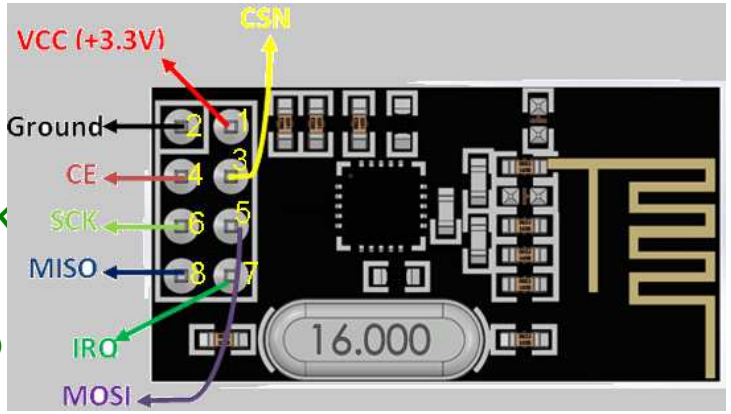


Possible SPI peripherals:
1) NRF24L01 module
2) Anything else.

Radio_CE and Radio_IRQ are shared with the WiFi module. You can use either the one or the other.

NRF24L01+ module, top view





Pin out compatible with https://components101.com/wireless/nrf24l01-pinout-features-datasheet

+3.3V_D
GND

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

Title: Wireless module NRF24L01+ socket

Size	Document Number	Rev
A	RiskZero LX9 Single Board Workstation Computer	0.1

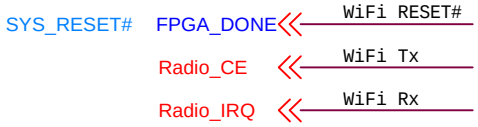
Date: Tuesday, September 29, 2020 Sheet 19 of 40

Connector for WiFi Sparkfun WRL-13678

The socket pinout is compatible with the WRL-13678.
It is mutually exclusive with the Nordic NFR24L01+

https://www.digikey.com/products/en?keywords=1568-1235-ND ← **How to purchase the WiFi module**

Due to pin shortage, these signals are reused from the Nordic radio in new roles.



Radio_CE and Radio_IRQ are shared with the Nordic module. You can use either the one or the other.

WRL-13678 module, top view

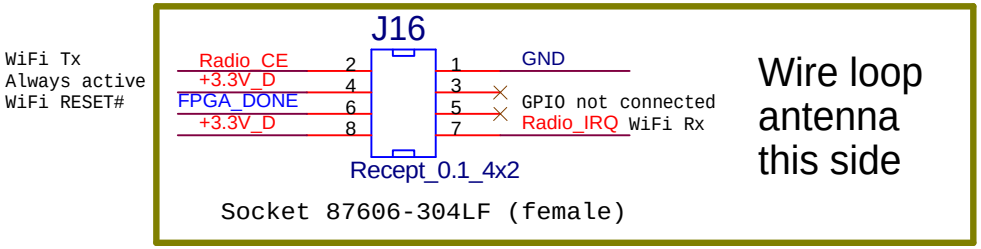


Figure copied from the DigiKey WRL-13678 datasheet, part number 1568-1235-ND
See also https://github.com/esp8266/esp8266-wiki/wiki/Hardware_versions

+3.3V_D

GND

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687		
Title: Wireless WiFi module WRL-13678 socket		
Size: A	Document Number: RiskZero LX9 Single Board Workstation Computer	Rev: 0.1
Date: Tuesday, September 29, 2020	Sheet 20 of 40	

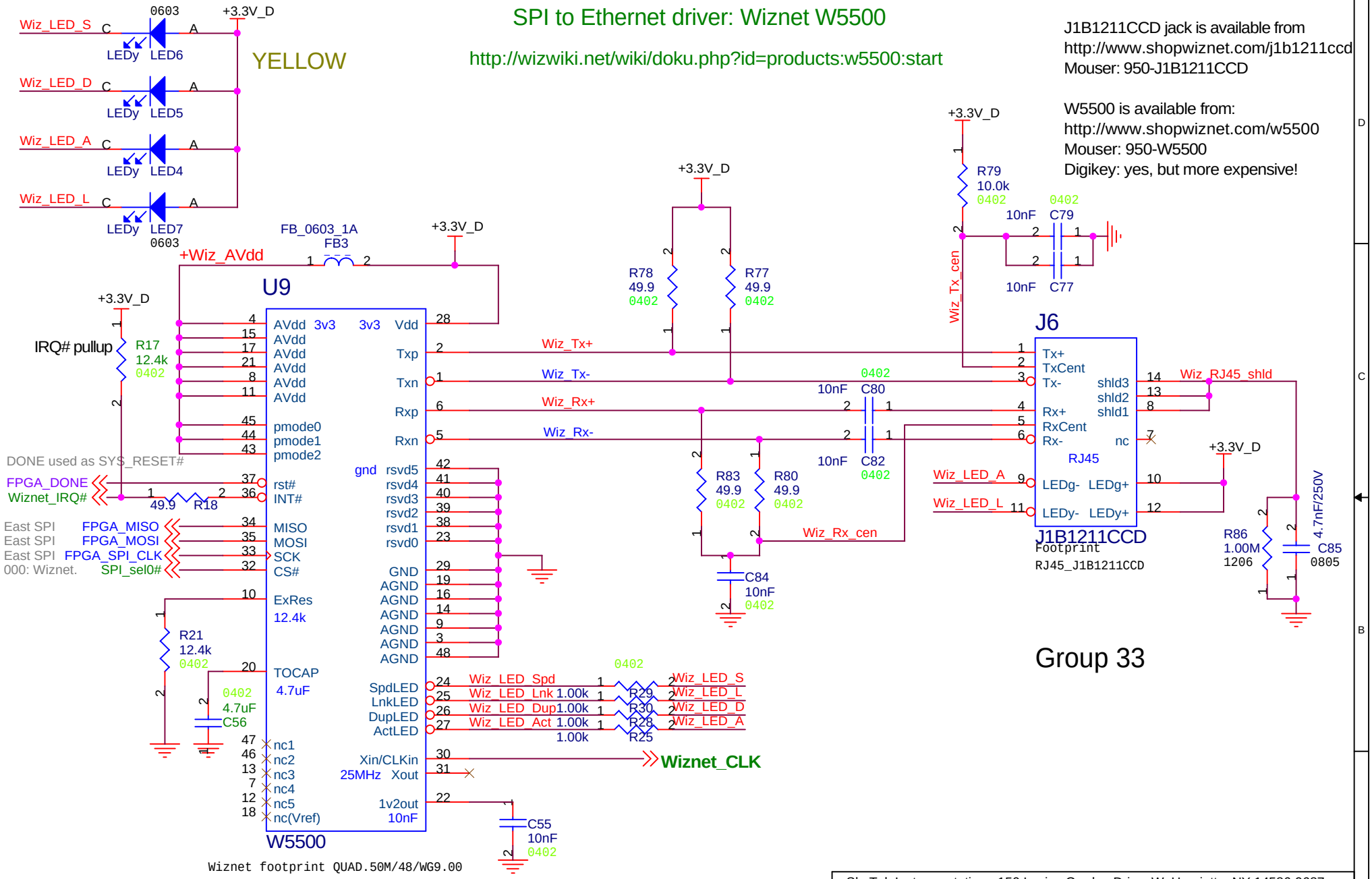
SPI to Ethernet driver: Wiznet W5500

http://wizwiki.net/wiki/doku.php?id=products:w5500:start

J1B1211CCD jack is available from
http://www.shopwiznet.com/j1b1211ccd
Mouser: 950-J1B1211CCD

W5500 is available from:
http://www.shopwiznet.com/w5500
Mouser: 950-W5500
Digikey: yes, but more expensive!

Group 33



SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687		
Title: Wiznet W5500 SPI to Ethernet interface		
Size: A	Document Number: RiskZero LX9 Single Board Workstation Computer	Rev: 0.1
Date: Tuesday, September 29, 2020	Sheet 21 of 40	

ZBT SRAM 2 * 512k * 36 bits

ZBT_ben_[0:3]
ZBT_A[0:18]
ZBT_data[0:31]

ZBT_CS Chip select
ZBT_clk
ZBT_R_W#
ZBT_adv_LD#

U11

ZBT_A6 ZBT_A7 GND ZBT_CS ZBT_ben_3 ZBT_ben_2 ZBT_ben_1 ZBT_ben_0 GND Vdd GND ZBT_clk ZBT_R_W# GND GND ZBT_adv_LD# ZBT_A18 ZBT_A17 ZBT_A8 ZBT_A9

1	ZBT0_P3	ioP3	
2	ZBT_DATA16	io16	
3	ZBT_DATA17	io17	
4	Vdd	vddq	
5	GND	vss	
6	ZBT_DATA18	io18	
7	ZBT_DATA19	io19	
8	ZBT_DATA20	io20	
9	ZBT_DATA21	io21	
10	GND	vss	
11	Vdd	vddq	
12	ZBT_DATA22	io22	
13	ZBT_DATA23	io23	
14	Vdd	vdd	
15	Vdd	vdd	
16	Vdd	vdd	
17	GND	vss	
18	ZBT_DATA24	io24	
19	ZBT_DATA25	io25	
20	Vdd	vddq	
21	GND	vss	
22	ZBT_DATA26	io26	
23	ZBT_DATA27	io27	
24	ZBT_DATA28	io28	
25	ZBT_DATA29	io29	
26	GND	vss	
27	Vdd	vddq	
28	ZBT_DATA30	io30	
29	ZBT_DATA31	io31	
30	ZBT0_P4	ioP4	

80	ZBT0_P2	ioP2	
79	ZBT_DATA15	io15	
78	ZBT_DATA14	io14	
77	Vdd	vddq	
76	GND	vss	
75	ZBT_DATA13	io13	
74	ZBT_DATA12	io12	
73	ZBT_DATA11	io11	
72	ZBT_DATA10	io10	
71	GND	vss	
70	Vdd	vddq	
69	ZBT_DATA9	io9	
68	ZBT_DATA8	io8	
67	GND	vss	
66	Vdd	vdd	
65	Vdd	vdd	
64	ZBT_ZZ	ZZ	
63	ZBT_DATA7	io7	
62	ZBT_DATA6	io6	
61	Vdd	vddq	
60	GND	vss	
59	ZBT_DATA5	io5	
58	ZBT_DATA4	io4	
57	ZBT_DATA3	io3	
56	ZBT_DATA2	io2	
55	GND	vss	
54	Vdd	vddq	
53	ZBT_DATA1	io1	
52	ZBT_DATA0	io0	
51	ZBT0_P1	ioP1	

a6 a7 ce1# ce2 bw4# bw3# bw2# bw1# ce2# vdd vss CLK R/W CEN# OE# adv / LD# a18 a17 a8 a9

LBO a5 a4 a3 a2 a1 a0 tms (nc) tdi (nc) vss vdd tdo (nc) tck (nc) a10 a11 a12 a13 a14 a15 a16

Use the part with correct Vcc!

ZBT SRAM
TQFP-100
14 x 22 mm

OE# always enabled

Group 30

3.3V

ISSI

IS61NLP51236B-200TQL

The parity bits are not used.

OE# always enabled
Data Sheet p.2

U14

ZBT_A6 ZBT_A7 GND Vdd ZBT_ben_3 ZBT_ben_2 ZBT_ben_1 ZBT_ben_0 ZBT_CS Vdd GND ZBT_R_W# GND GND ZBT_adv_LD# ZBT_A18 ZBT_A17 ZBT_A8 ZBT_A9

1	ZBT1_P3	ioP3	
2	ZBT_DATA16	io16	
3	ZBT_DATA17	io17	
4	Vdd	vddq	
5	GND	vss	
6	ZBT_DATA18	io18	
7	ZBT_DATA19	io19	
8	ZBT_DATA20	io20	
9	ZBT_DATA21	io21	
10	GND	vss	
11	Vdd	vddq	
12	ZBT_DATA22	io22	
13	ZBT_DATA23	io23	
14	Vdd	vdd	
15	Vdd	vdd	
16	Vdd	vdd	
17	GND	vss	
18	ZBT_DATA24	io24	
19	ZBT_DATA25	io25	
20	Vdd	vddq	
21	GND	vss	
22	ZBT_DATA26	io26	
23	ZBT_DATA27	io27	
24	ZBT_DATA28	io28	
25	ZBT_DATA29	io29	
26	GND	vss	
27	Vdd	vddq	
28	ZBT_DATA30	io30	
29	ZBT_DATA31	io31	
30	ZBT1_P4	ioP4	

80	ZBT1_P2	ioP2	
79	ZBT_DATA15	io15	
78	ZBT_DATA14	io14	
77	Vdd	vddq	
76	GND	vss	
75	ZBT_DATA13	io13	
74	ZBT_DATA12	io12	
73	ZBT_DATA11	io11	
72	ZBT_DATA10	io10	
71	GND	vss	
70	Vdd	vddq	
69	ZBT_DATA9	io9	
68	ZBT_DATA8	io8	
67	GND	vss	
66	Vdd	vdd	
65	Vdd	vdd	
64	ZBT_ZZ	ZZ	
63	ZBT_DATA7	io7	
62	ZBT_DATA6	io6	
61	Vdd	vddq	
60	GND	vss	
59	ZBT_DATA5	io5	
58	ZBT_DATA4	io4	
57	ZBT_DATA3	io3	
56	ZBT_DATA2	io2	
55	GND	vss	
54	Vdd	vddq	
53	ZBT_DATA1	io1	
52	ZBT_DATA0	io0	
51	ZBT1_P1	ioP1	

a6 a7 ce1# ce2 bw4# bw3# bw2# bw1# ce2# vdd vss CLK R/W CEN# OE# adv / LD# a18 a17 a8 a9

LBO a5 a4 a3 a2 a1 a0 tms (nc) tdi (nc) vss vdd tdo (nc) tck (nc) a10 a11 a12 a13 a14 a15 a16

Use the part with correct Vcc!

ZBT SRAM
TQFP-100
14 x 22 mm

OE# always enabled

Group 29

3.3V

ISSI

IS61NLP51236B-200TQL

The parity bits are not used.

0402
1 49.9 2 R82
ZBT_clk

Place at far end.
Use high current drive.

+3.3V_D
R22 12.4k 0402
ZBT_LBO

JP2
JUMPER_0_1

Linear Burst Order LBO is static. Must not change.
Choose HIGH / LOW according to the Data Sheet.

Turn the chips off

+3.3V_D Vdd
GND
ZBT_ZZ
JP3
JUMPER_0_1

Manufacturer Part Number
IS61NLP51236B-200TQL
SRAM 18MBIT 3.3V
200 MHz 100TQFP
Mouser: 39 on
Aug/21/2020

Group 30

ZBT0_P3 R23 12.4k 0402
ZBT0_P4 R24 12.4k 0402
ZBT0_P1 R16 12.4k 0402
ZBT0_P2 R19 12.4k 0402

Group 29

ZBT1_P3 R31 12.4k 0402
ZBT1_P4 R32 12.4k 0402
ZBT1_P1 R27 12.4k 0402
ZBT1_P2 R26 12.4k 0402

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687

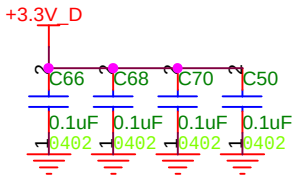
Title
ZBT memory; two chips

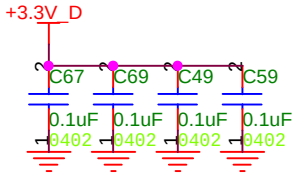
Size A
Document Number
RiskZero LX9 Single Board Workstation Computer
Rev 0.1

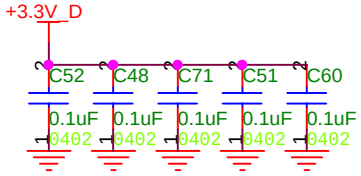
Date: Tuesday, September 29, 2020 Sheet 22 of 40

ZBT chip 1

Group 30

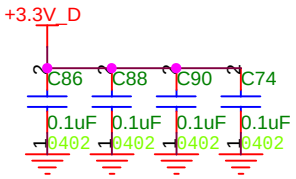


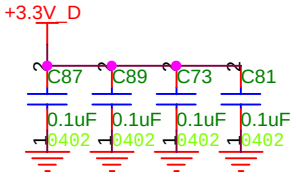


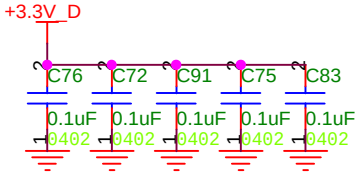


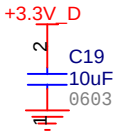
ZBT chip 2

Group 29



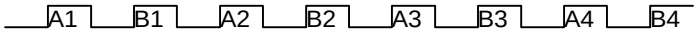






Notes

The pipelined ZBT works with 2 clock cycle latency in both read and write cycles. In the write direction, the address is presented at A1. The data is expected by the ZBT chip at A2. The cycle B1 should be skipped. The same is true with reading from the chip.



The figure shows that the interleaved A and B cycles effectively define a dual-port operation, when the ZBT runs at twice the clock frequency of the bus host. There are three possible use cases.

1. The cycles A are used and B are discarded. The ZBT becomes a single port memory much like ASRAM. The ASRAM memory controller can be used with little modification.

2. Two bus hosts can access memory at A or B cycles without disrupting each other. The ZBT is operated as a dual port memory, with ports A and B operating at the alternating clocks.

3. The controller is using a single port at the full bandwidth w/o the regard to two-clock latency. The controller is internally pipelining the data to generate the needed two-clock "misalignment". Both the Xilinx and Altera cores are doing just that (see below).

Open Cores implementation of the dual-port design is available in VHDL. It is pretty old (2001). Presumably it can be adopted to Spartan-6 with only moderate effort.

https://opencores.org/projects/ssram

Xilinx App Note XAPP136 (v2.0) January 10, 2000 titled "Synthesizable 200 MHz ZBT SRAM Interface" describes ZBT and its controller. This App Note is marked "obsolete", but I see no reason to disregard the implementation.

A similar note AN-329-1.0 is available from Altera, titled "ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices".

Neither Xilinx nor Altera discuss the dual-port use of the ZBT chip. They are rather maximizing the throughput by internally "misaligning" the address and the data. These controllers would be needed if the soft CPU could run at 200 MHz.

Note that Spartan-6 on-chip hardened memory interface does not support ZBT. It is thus not clear why XAPP136 was marked "obsolete".

SkuTek Instrumentation - 150 Lucius Gordon Drive, W. Henrietta, NY 14586-9687		
Title: ZBT decoupling capacitors		
Size: A	Document Number: RiskZero LX9 Single Board Workstation Computer	Rev: 0.1
Date: Tuesday, September 29, 2020	Sheet 23 of 40	