RiskFive FPGA Module Development Motherboard. ZBT Version.

REV	Description	DATE	BY
0	PRELIMINARY prototype release for review. Not manufactured yet.	07/24/2018.	ws
1			
2			

07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.

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West Henrietta, NY 14586 - 9687
http://www.skutek.com

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NORTH header

DOWN inside brd

JH1A

UP outside brd

Bank 14
3.3V

K18 (Bank 14) XSPI_miso
K17 (Bank 14) XSPI_mosi
L14 (Bank 14) XSPI_D2
M14 (Bank 14) XSPI_D3
E9 & L16 (0 & 14) XSPI_CCLK

	K18 (Bank 14)		1	80	POWER OFF/ON		
	K17 (Bank 14)		2	79	P9 Bank 0		
	L14 (Bank 14)		3	78	P10 Bank 0		
	M14 (Bank 14)		4	77	IRQ_Radio	IO_15_L23P_j17	
	E9 & L16 (0 & 14)		5	76	IRQ_I2C#	IO_15_L23N_j18	
Bank 14 3.3V	IO_14_L22P_u14	W5300_A6	6	75	IRQ_Soft#	IO_15_0_g13	
	IO_14_L22N_v14	W5300_A7	7	74	W5300_A5	IO_14_L15P_r16	
	IO_14_L23P_t13	W5300_A8	8	73	W5300_A4	IO_14_L15N_t16	
	IO_14_L23N_u13	W5300_A9	9	72	W5300_A3	IO_14_L14P_t14	
	IO_14_L20P_u12	W5300_D0	10	71	W5300_A2	IO_14_L14N_t15	
	IO_14_L20N_v12	W5300_D1	11	70	W5300_A1	IO_14_L8P_n14	
	IO_14_L5P_r12	W5300_D2	12	69	W5300_WR#	IO_14_L8N_p14	
	IO_14_L5N_r13	W5300_D3	13	68	SOFT_Reset#	IO_14_0_r11 (single)	
	IO_14_L19P_t11	W5300_D4	14	67	W5300_RD#	IO_14_L24P_t9	
	IO_14_L19N_u11	W5300_D5	15	66	W5300_CS#	IO_14_L24N_t10	
	IO_14_L21P_v10	W5300_D6	16	65	IRQ_W5300#	IO_34_L21P_u9	
	IO_14_L21N_v11	W5300_D7	17	64	W5300_brdy0	IO_34_L21N_v9	
	IO_14_25_r10 (sng)	W5300_D8	18	63	W5300_brdy1	IO_34_25_U8 (single)	
	IO_34_L24P_r8	W5300_D9	19	62	W5300_brdy2	IO_34_L23p_r7	
	IO_34_L24N_t8	W5300_D10	20	61	W5300_brdy3	IO_34_L23n_t6	
	IO_34_L20P_v7	W5300_D11	21	60	VGA_red0	IO_34_L22P_u7	
	IO_34_L20N_v6	W5300_D12	22	59	VGA_red1	IO_34_L22N_u6	
	IO_34_L19p_r6	W5300_D13	23	58	VGA_red2	IO_34_L13p_n5	
	IO_34_L19n_r5	W5300_D14	24	57	VGA_red3	IO_34_L13n_p5	
	IO_34_L10P_v5	W5300_D15	25	56	VGA_red4	IO_34_L8p_u4	
	IO_34_L10N_v4	VGA_grn0	26	55	VGA_red5	IO_34_L8n_u3	
	IO_34_L12P_t5	VGA_grn1	27	54	VGA_red6	IO_34_L6p_L6	
	IO_34_L12N_t4	VGA_grn2	28	53	VGA_red7	IO_34_L6n_L5	
	IO_34_L11p_r3	VGA_grn3	29	52	VGA_blank#	IO_34_L14p_p4	
	IO_34_L11n_t3	VGA_grn4	30	51	VGA_sync#	IO_34_L14n_p3	
Bank 34 3.3V	IO_34_L9p_u2	VGA_grn5	31	50	VGA_blue0	IO_34_L15p_p2	
	IO_34_L9N_v2	VGA_grn6	32	49	VGA_blue1	IO_34_L15n_r2	
	IO_34_L7p_u1	VGA_grn7	33	48	VGA_blue2	IO_34_L17p_r1	
	IO_34_L7n_v1	VGA_blue4	34	47	VGA_blue3	IO_34_L17n_t1	
	IO_34_L18p_m6	VGA_blue5	35	46	SD_DATA1	IO_16_L19N_d10	
	IO_34_L18n_n6	VGA_blue6	36	45	SD_DATA0	IO_16_L6N_d9	
	IO_34_L3p_n2	VGA_blue7	37	44	SD_CLK	IO_16_L11P_c9	
	IO_34_L3n_n1	VGA_pix_clk	38	43	SD_CMD_din	IO_16_L11N_b9	
	IO_34_L4p_m3	VGA_HSYNC	39	42	SD_DATA3_CS#	IO_16_L12P_b8	
	IO_34_L4n_m2	VGA_VSYNC	40	41	SD_DATA2	IO_16_L12N_a8	

POWER_ON HIGH to Enable 3.3V power
X_PRGM# P9 FPGA conf
X_DONE P10 FPGA conf
Bank 0

Bank 15 variable Vcco=3.3V

Bank 14
3.3V

Bank 34
3.3V

Bank 16
variable
Vcco=3.3V

FX11LA-80S/8-SV(71)

Footprint FX11L80/H/GP

Power Cycle SW4

POWER_ON — 4 3 2 1 — Switch_6mm

FPGA Reload SW1

X_PRGM# — 4 3 2 1 — Switch_6mm

SD card

SD_DATA1
SD_DATA0
SD_CLK
SD_CMD_din
SD_DATA3_CS#
SD_DATA2

Ethernet chip

IRQ_W5300#
W5300_WR#
W5300_RD#
W5300_CS#
W5300_brdy[3:0]
W5300_A[9:1]
W5300_D[15:0]

VGA Video DAC

VGA_red[0:7]
VGA_grn[0:7]
VGA_blue[0:7]
VGA_blank#
VGA_sync#
VGA_pix_clk

VGA Logic

VGA_HSYNC
VGA_VSYNC
VGA_SCL
VGA_SDA

Soft CPU signals

SOFT_Reset#
IRQ_Soft#

I2C Expander

IO_15_L23N_j18 IRQ_I2C#

Radio

IO_15_L23P_j17 IRQ_Radio
active HIGH

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Footprint FX11L80/R/GP

CONN HEADER 80POS W/POSTS SMD
FX11LA-80P/8-SV(71) -> mezzanine

CONN RECEPT 80POS W/POSTS SMD
FX11LA-80S/8-SV(71) ->
motherboard

sh1 sh2 sh3 sh4 sh5 Post1 — JH1B — END1 END2 sh8 sh7 sh6 Post2

FX11LA-80S/8-SV(71)

GND

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SOUTH header

DOWN outside brd

UP inside brd

JH2A

Ether activity	Ether_LED0	GbE	1	1	80	GbE		Ether_LED1	Ether activity
GbE	Ether2+	GbE	2	2	79	GbE		Ether0+	GbE
GbE	Ether2-	GbE	3	3	78	GbE		Ether0-	GbE
GbE	Ether3+	GbE	4	4	77	GbE		Ether1+	GbE
GbE	Ether3-	GbE	5	5	76	GbE		Ether1-	GbE
		EXP_strobe_0	6	6	75	PS2_clk1	IO_15_L24P_k15		
Signals from I2C Expander		EXP_strobe_1	7	7	74	PS2_d1	IO_15_L24N_j15		
		EXP_strobe_2	8	8	73	PS2_d2	IO_15_L18P_h17		
I2C_data	I2C_d	IO_14_L13N_r15	9	9	72	PS2_clk2	IO_15_L18N_g17		
I2C_clk	I2C_c	IO_14_L6N_m13	10	10	71	W5500_MOSI	IO_15_L16P_e17		
UART_Rx	Rx	IO_14_L12N_r17	11	11	70	W5500_SPI_CLK	IO_15_L16N_d17		
UART_Tx	Tx	IO_14_L3P_PUDC_L15	12	12	69	W5500_MISO	IO_15_25_k16 sngl		
PMOD_EN_0	RTS	IO_14_L10P_m16	13	13	68	W5500_CS#	IO_15_L20P_c16		
PMOD_EN_1	CTS	IO_14_L10N_m17	14	14	67	IRQ_W5500#	IO_15_L20N_c17		
FT601_D13		IO_14_L9P_n17	15	15	66	FT601_D0	IO_15_L3P_c12		
FT601_D14		IO_14_L9N_p18	16	16	65	FT601_D1	IO_15_L3N_b12		
FT601_D15		IO_14_L4P_L18	17	17	64	FT601_D2	IO_15_L14P_f15 srcc+		
FT601_D16		IO_14_L4N_m18	18	18	63	FT601_D3	IO_15_L14N_f16 srcc-		
FT601_D17		IO_14_L11P_n15	19	19	62	FT601_D4	IO_15_L10P_b18		
FT601_D18		IO_14_L11N_n16	20	20	61	FT601_D5	IO_15_L10N_a18		
FT601_D19		IO_15_L19P_j14	21	21	60	FT601_D6	IO_15_L2P_b13		
FT601_D20		IO_15_L19N_h15	22	22	59	FT601_D7	IO_15_L2N_b14		
FT601_D21		IO_15_L17P_k13	23	23	58	FT601_D8	IO_15_L9P_a13		
FT601_D22		IO_15_L17N_j13	24	24	57	FT601_D9	IO_15_L9N_a14		
FT601_D23		IO_15_L15P_h14	25	25	56	FT601_D10	IO_15_L4P_b11		
FT601_D24		IO_15_L15N_g14	26	26	55	FT601_D11	IO_15_L4N_a11		
FT601_CLK_out		IO_15_L13P_h16 mrcc+	27	27	54	FT601_D12	IO_15_L8P_a15		
FT601_D25		IO_15_L13N_g16 mrcc-	28	28	53	FT601_D31	IO_15_L8N_a16		
FT601_D26		IO_15_L22P_g18	29	29	52	FT601_OE#	IO_15_L7P_b16		
FT601_D27		IO_15_L22N_f18	30	30	51	FT601_Wakeup#	IO_15_L7N_b17		
FT601_D28		IO_15_L5P_f13	31	31	50	FT601_GPIO0	IO_15_L12P_d15 mrcc+		
FT601_D29		IO_15_L5N_f14	32	32	49	FT601_GPIO1	IO_15_L12N_c15 mrcc-		
FT601_D30		IO_15_L1P_d14	33	33	48	PMOD_GPIO_0	IO_16_L13P_c11 mrcc+		
FT601_BE0		IO_15_L1N_c14	34	34	47	PMOD_GPIO_1	IO_16_L13N_c10 mrcc-		
FT601_BE1		IO_15_L11P_e15 srcc+	35	35	46	PMOD_GPIO_2	IO_16_L14P_a10 srcc+		
FT601_BE2		IO_15_L11N_e16 srcc-	36	36	45	PMOD_GPIO_3	IO_16_L14N_a9 srcc-		
FT601_BE3		IO_15_L21P_e18	37	37	44	XTMS	in		
FT601_Tx_empty#		IO_15_L21N_d18	38	38	43	XTDI	in		
FT601_Rx_full#		IO_15_L6P_d12	39	39	42	XTDO	out		
FT601_WR#		IO_15_L6N_d13	40	40	41	XTCK	in		

FX11LA-80S/8-SV(71)

I2C
UART

Bank 14
3.3V

Bank 15
variable
Vcco=3.3V

66 or 100 MHz
to FPGA

Bank 15
variable
Vcco=3.3V

Bank 16
variable
Vcco=3.3V

FT_GPIO pins are power on mode pins for the FT60x chip

CTS, RTS reserved on Abone, but not really used.

UART_Tx → UART_chip_Tx → To RS-232
UART_Rx → UART_chip_Rx → From RS-232

SD_card_prot — Full size

SD_DATA1
SD_DATA0
SD_CLK
SD_CMD_din
SD_DATA3_CS#
SD_DATA2
— Both micro and full

W5300 is on
North Hirose

IRQ_W5500#
SPI W5500_MISO
SPI W5500_MOSI
SPI W5500_SPI_CLK
Chip sel W5500_CS#

HW Chip Strobe or Reset
From I2C Expander EXP_strobe_[0:2]

I2C — I2C_data, I2C_clk

PS/2 — PS2_clk1, PS2_d1, PS2_d2, PS2_clk2

USB-3
FT601_D[31:0]
FT601_BE[3:0]
FT601_Tx_empty#
FT601_Rx_full#
45
FT601_WR#
FT601_RD#
FT601_OE#
FT601_WAKEUP#
Boot mode
FT601_GPIO0
FT601_GPIO1
FT601_CLK_out

PMOD Enable signals
PMOD_EN_[0:1]
RTS/CTS are alternative

Fast PMOD
S.Hirose PMOD_GPIO_[0:3]
Also used for wireless module

Footprint FX11L80/R/GP

CONN HEADER 80POS W/POSTS SMD
FX11LA-80P/8-SV(71) -> mezzanine

CONN RECEPT 80POS W/POSTS SMD
FX11LA-80S/8-SV(71) ->
motherboard

JH2B

sh1 sh2 sh3 sh4 sh5 Post1 — END1 END2 sh8 sh7 sh6 Post2

FX11LA-80S/8-SV(71)

GND GND

JTAG
J16

XTDI	TDI	14	13
XTDO	TDO	12	11
XTCK	TCK	10	9
XTMS	TMS	8	7
+3.3V_D		6	5
		4	3
		2	1

CON14A
Molex 0878311420
WM17469-ND

+3.3V_D
GND
GND

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MBone connectors

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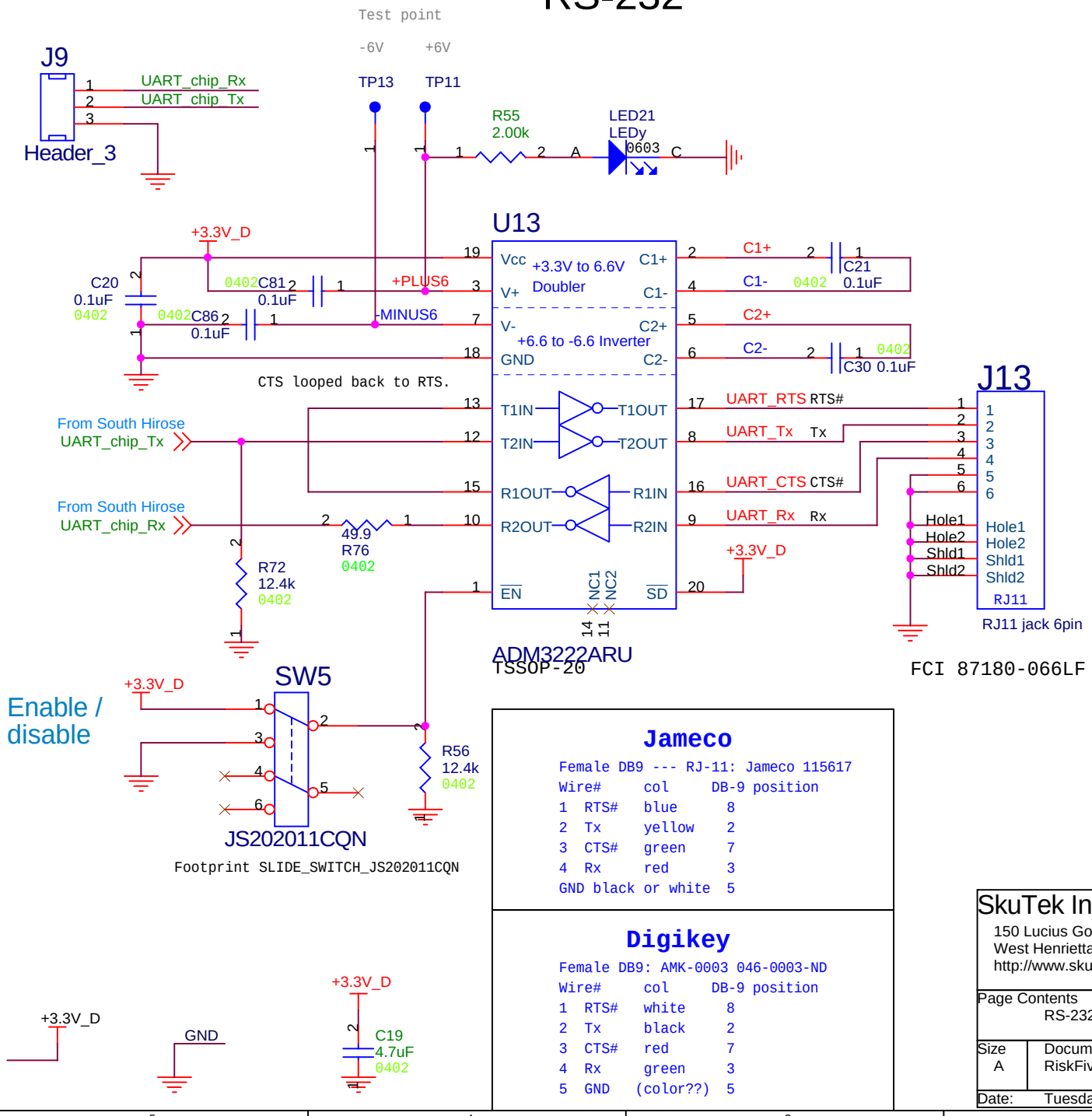
Pin header for the FTDI USB-UART cable. While using the FTDI the RS232 must be disabled.

RS-232



Jameco

Female DB9 --- RJ-11: Jameco 115617

Wire#	col	DB-9 position
1 RTS#	blue	8
2 Tx	yellow	2
3 CTS#	green	7
4 Rx	red	3
GND	black or white	5

Digikey

Female DB9: AMK-0003 046-0003-ND

Wire#	col	DB-9 position
1 RTS#	white	8
2 Tx	black	2
3 CTS#	red	7
4 Rx	green	3
5 GND	(color??)	5

DB9 pin description

pin	PC(DTE) Function	BF Function
3	Transmit Data	Rx
2	Receive Data	Tx
7	Request to Send	RTS#
8	Clear to Send	CTS#

Software flow control is expected because CTS and RTS are looped back.

On-board RS-232 modular jack

A DB9 connector is too large for the board. Telephone-style jack with 6 pins is used instead. RS-232 pins are not assigned for such jacks. A configurable adapter is used to reassign the pins after the board is deployed.

TYCO RJ11-6Nxxxx $5 (about)
FCI 87180-066LF 609-1057-ND $1.41

Configurable adapter RJ11 --> DB9 by CUI
Male DB9: AMK-0002 046-0002-ND $4.13
Female DB9: AMK-0003 046-0003-ND $4.13

Jameco part numbers (six wire):
66203 Mfg: 31D1-16400-R $2.79

RJ cable

6-wire RJ cable between the adapter and the jack from I.O. Interconnect:

2.1m GLF-466-076-510-D H1663R-07-ND $3.34
7.6m GLF-466-256-511-D H1662R-25-ND $5.54

Jameco part number (7 feet, six wires 6P6C):
115617 Mfg: 306-707SL $1.99

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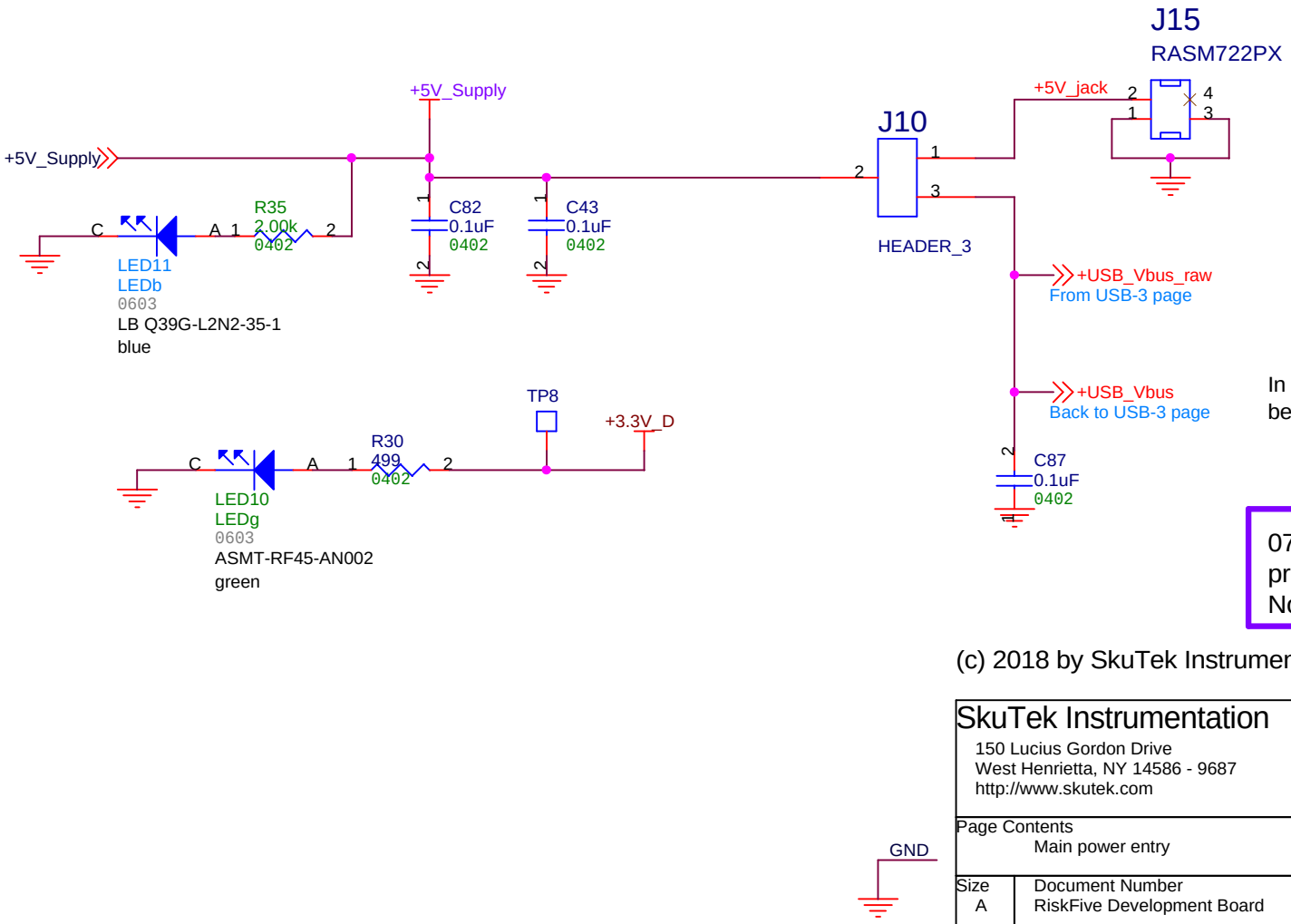
Power entry for the motherboard

RASM712PX = CONN JACK R/A .100" PIN SMD (2.5mm)
RASM722PX = CONN JACK R/A .080" PIN SMD (2.1mm)
P means locating post as an option
Contact rating: 3A

Recommended power supplies from Jameco with 2.1 mm:
379623 Mean Well GS25U05-P1J 5V/4A
1952863 Mean Well GS18U05-P1J 5A/3A

Recommended power supplies from Jameco with 2.5 mm:
2167664 FAIRWAY WN20U-050 5V/3A



In principle, I could filter Vbus with a bead, but I chose not to.

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Main power entry

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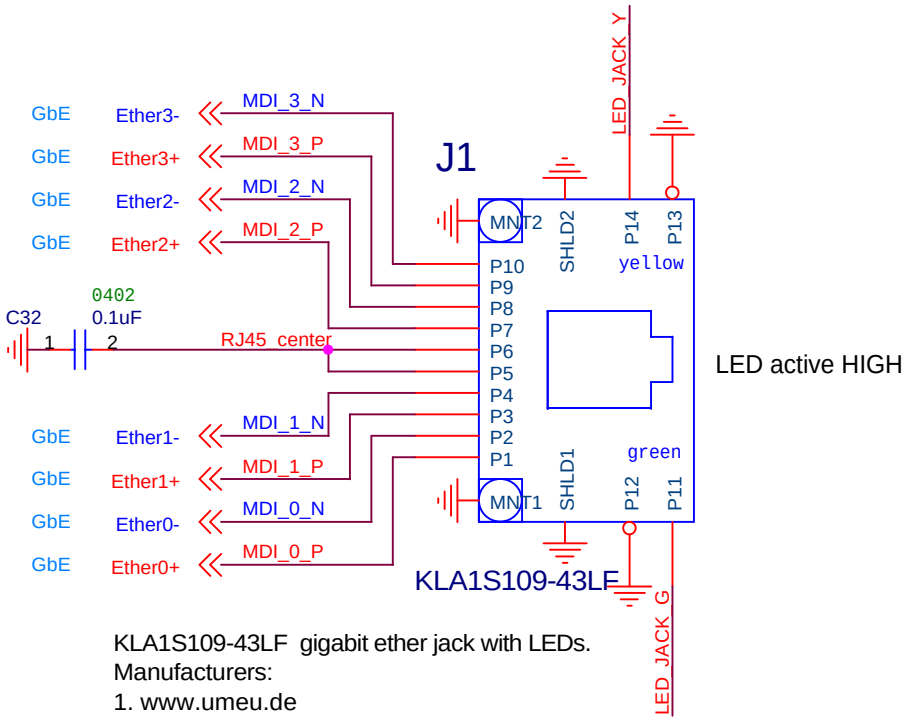
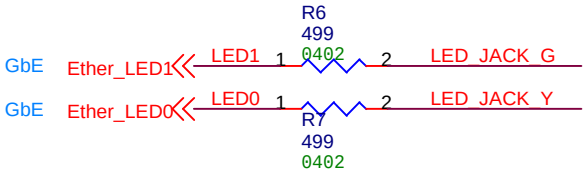
GbE jack



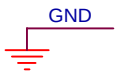
LED active HIGH

KLA1S109-43LF gigabit ether jack with LEDs.
Manufacturers:
1. www.umeu.de
2. www.bothhandusa.com

Center tap to AVdd not required. Internal on-chip termination provided on Media Dependent Interface (i.e., magnetics).



LED active HIGH



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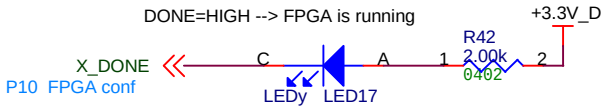
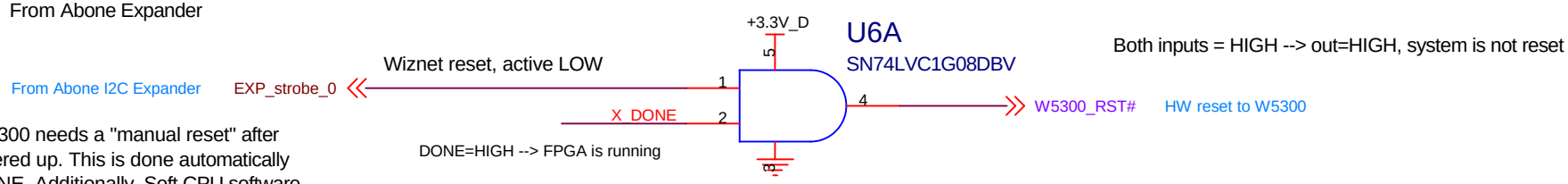
Reset generators

Due to shortage of FPGA pins we use I2C Expander to route three active low strobes. (They are also driving LEDs on the Abone). The strobes are or'ed with manual pushbuttons.

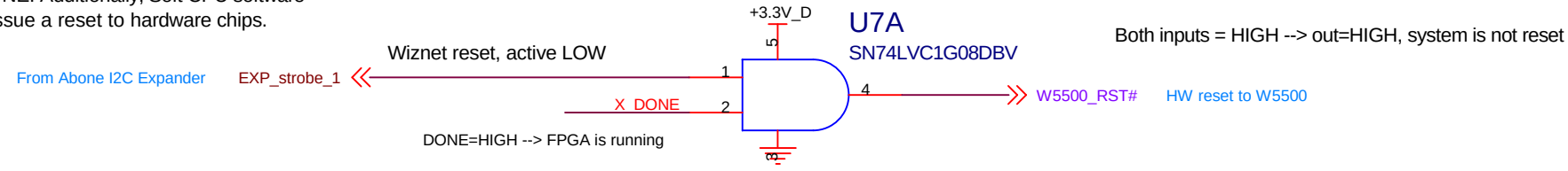
U6B
SN74LVC1G08DBV
SOT-23-5

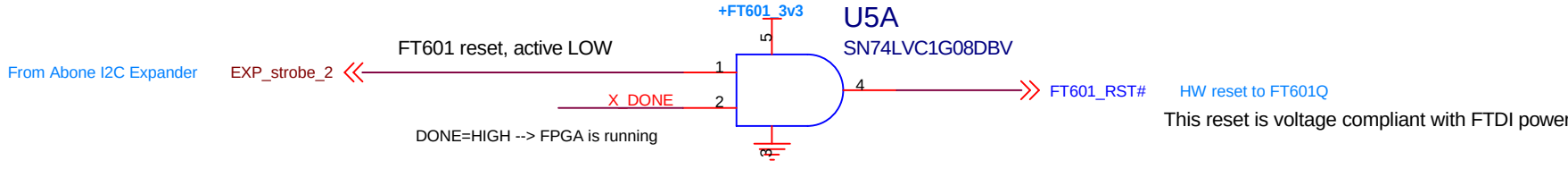


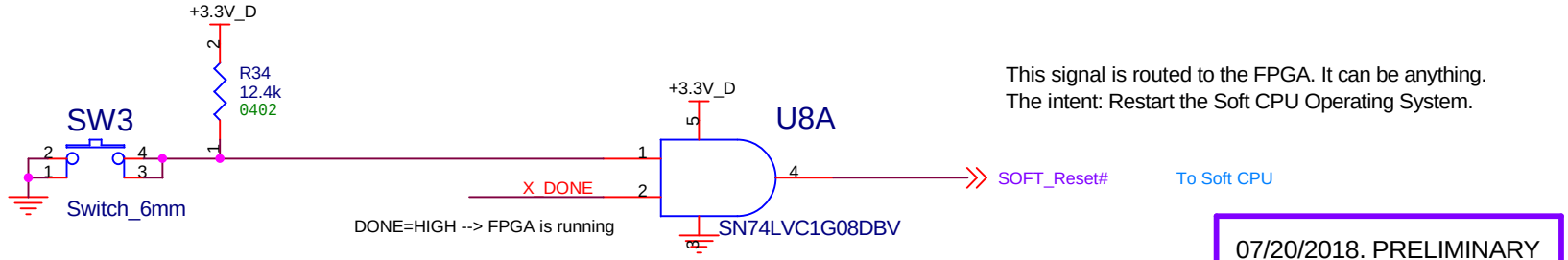
From Abone Expander



Wiznet W5300 needs a "manual reset" after being powered up. This is done automatically with X_DONE. Additionally, Soft CPU software can also issue a reset to hardware chips.







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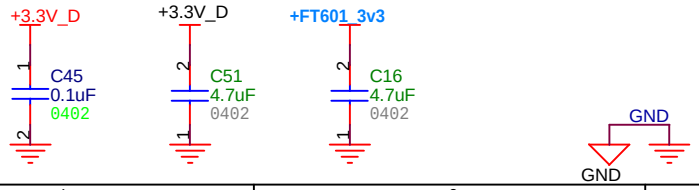
Group 13



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South LED display

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USB3 chip FT601Q

Footprint QFN-76_FT601Q_12_vias

+Vcco_var +FT601_3v3 FT601 is connected to Banks 15,16

U3A

FT601Q USB3 1/5

FT601_D31 76 D31
FT601_D30 75 D30
FT601_D29 74 D29
FT601_D28 73 D28
FT601_D27 72 D27
FT601_D26 71 D26
FT601_D25 70 D25
FT601_D24 69 D24
FT601_D23 67 D23
FT601_D22 66 D22
FT601_D21 65 D21
FT601_D20 64 D20
FT601_D19 63 D19
FT601_D18 62 D18
FT601_D17 61 D17
FT601_D16 60 D16
FT601_D15 57 D15
FT601_D14 56 D14
FT601_D13 55 D13
FT601_D12 54 D12
FT601_D11 53 D11
FT601_D10 52 D10
FT601_D9 51 D9
FT601_D8 50 D8
FT601_D7 47 D7
FT601_D6 46 D6
FT601_D5 45 D5
FT601_D4 44 D4
FT601_D3 43 D3
FT601_D2 42 D2
FT601_D1 41 D1
FT601_D0 40 D0

FT601_BE0 4 BE_0
FT601_BE1 5 BE_1
FT601_BE2 6 BE_2
FT601_BE3 7 BE_3

FT601Q-B-T

45 pins

FT601_D[31:0]
FT601_BE[3:0]

U3E

+FT601_1v0 +FT601_3v3

LDO_1v0_out 39
Vd_1v0_in 3
Vd_1v0_in 30
Vd_1v0_in 33
Vd_1v0_in 48
AVdd_1v0_in 2
gnd4 36
gnd3 29
gnd2 26
gnd1 1

VddA_3v3_in 28
Vcc33_in 38
Vcc33_in 20
Vcc33_in 24
VccIO_in 68
VccIO_in 59
VccIO_in 49
VccIO_in 14
88 87 86 85

77 78 79 80 81 82 83 84

FT601Q USB3 3/5
FT601Q-B-T

C10 4.7uF
C42 4.7uF

1.0V TP2

U3C

SIWU#_pullup 10
reserved (nc) 19
Xtal_in 21
Xtal_out 22
Rref_1.6k 27

R16 2.00k 0402
18pF C36 0402
Y1 ABM7-30.000MHZ-D2Y-T
18pF C37 0402
1.60k R8

FT601Q USB3 3/5
FT601Q-B-T

U3D

FT601Q USB3 4/5

Vbus_in 37
USB2_Dn 25
USB2_Dp 23
USB3_in- 34
USB3_in+ 35
USB3_out- 31
USB3_out+ 32

From PWR entry page +USB_Vbus
To PWR entry page +USB_Vbus_raw

USB2_D-
USB2_D+
USB3_Rx-
USB3_Rx+
USB3_out-
USB3_out+
0.1uF C33
0.1uF C34

Tx needs caps

FT601Q-B-T

J2 USB-3.0

Shield1 11
Vbus 1
USB2_D- 2
USB2_D+ 3
gnd 4
USB3_Rx- 5
USB3_Rx+ 6
USB3_gnd 7
USB3_Tx- 8
USB3_Tx+ 9
Shield2 10

GND
GND
USB3_Tx-
USB3_Tx+

USB 3.0 Connector
E8199-001-01

Crystals

ABM8G-30.000MHZ-18-D2Y-T
CRYSTAL 30.0000MHZ 18PF SMD four leads

ABM7-30.000MHZ-D2Y-T
535-9849-1-ND two leads; 1812

+FT601_1v0 0402
C13 C9 C5 C6 0.1uF

+FT601_3v3 0402
C88 C2 C4 C7 C12 C11 C8 C3 C1 0.1uF

U3B

FT601Q USB3 2/5

FT601_RST# 15 RESET#_in
FT601_WAKEUP# 16 Wakeup#
FT601_Tx_empty# 8 Tx_FIFO_Empty#
FT601_Rx_full# 9 Rx_FIFO_Full#
FT601_WR# 11 WR#_in
FT601_RD# 12 RD#_in
FT601_OE# 13 OE#_in
FT601_GPIO0 17 GPIO0
FT601_GPIO1 18 GPIO1
FT601_CLK_out 58 CLK_out

FT601Q-B-T

66 or 100 MHz

(GPIO1, GPIO0) boot strapping

(00) 1 channel, 245 Synchronous FIFO mode
(01) 1 channel, Multi-Channel FIFO mode
(10) 2 channel, Multi-Channel FIFO mode
(11) 4 channel, Multi-Channel FIFO mode

07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.

J17

FT601_GPIO0 2
HEADER_3
2.00k R5 +FT601_3v3
2.00k R4 GND
0402

J18

FT601_GPIO1 2
HEADER_3
2.00k R84 +FT601_3v3
2.00k R85 GND
0402

FT601_OE# 2.00k R10 +FT601_3v3
FT601_WR# 2.00k R13
FT601_RST# 2.00k R9
0402

GND

Group 1

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Page Contents: USB3

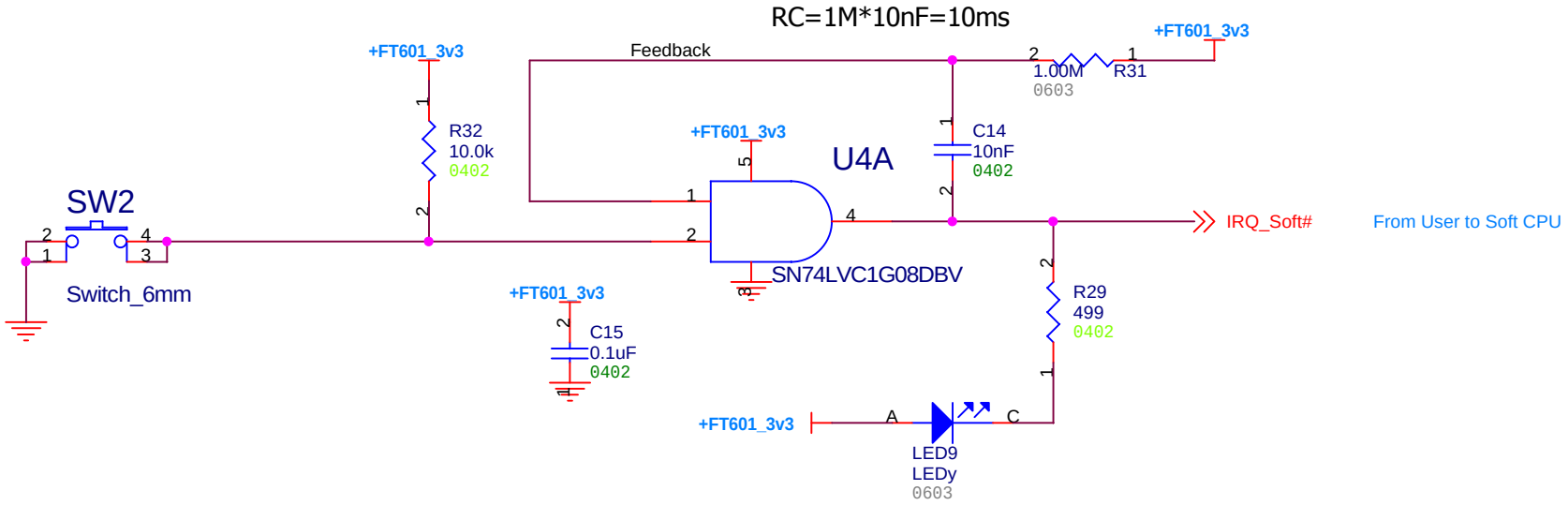
Size	Document Number	Rev
Custom	MicroBone Test Board	0

Date: Tuesday, July 24, 2018 Sheet 7 of 20

Push button and LED blinker

This circuit is a debouncer. FW debouncing is not needed.
Stationary output: HIGH. Push the button for LOW pulse.

This circuit is for manual interrupt generation and testing.



07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.

GND
GND

Group 4

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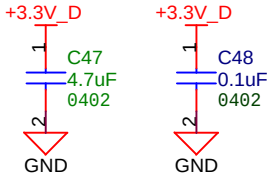
Page Contents
ADC test driven with the I2C0 test, and in/out for loopback tests

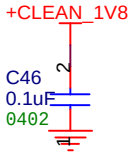
Size	Document Number	Rev
A	RiskFive Development Board	0

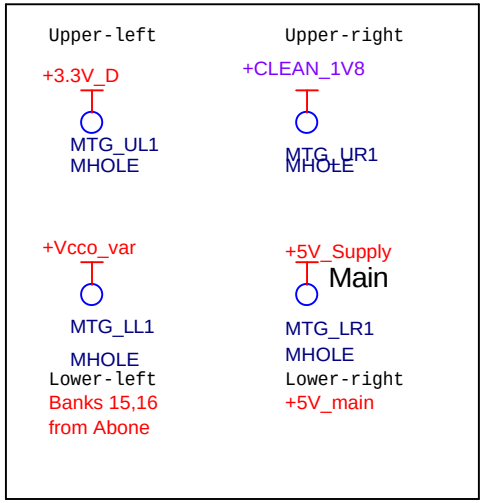
Date: Tuesday, July 24, 2018 Sheet 8 of 20

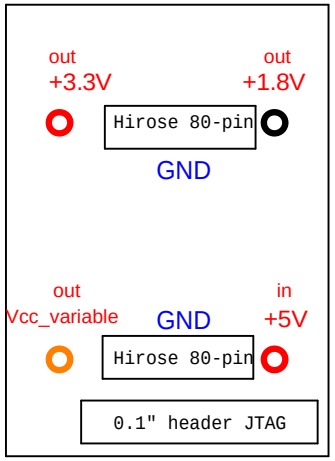
Power for the RiskFive ABone Rev 0 DUT

Board sketch



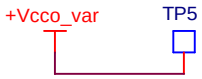




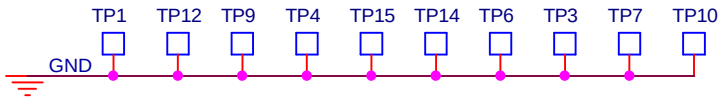


The board is powered with the lower-right mounting hole. Three other mounting holes are power outputs.

Hirose shields are ground.



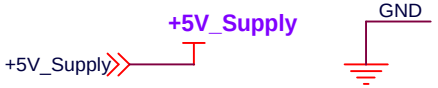
GND posts for attaching scope probes



Test point eyelets Keystone

5000	36-5000-ND	red
5001	36-5001-ND	black
5003	36-5003-ND	orange
5004	36-5004-ND	yellow
5117	36-5117-ND	blue

07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.



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Page Contents: Main power entry

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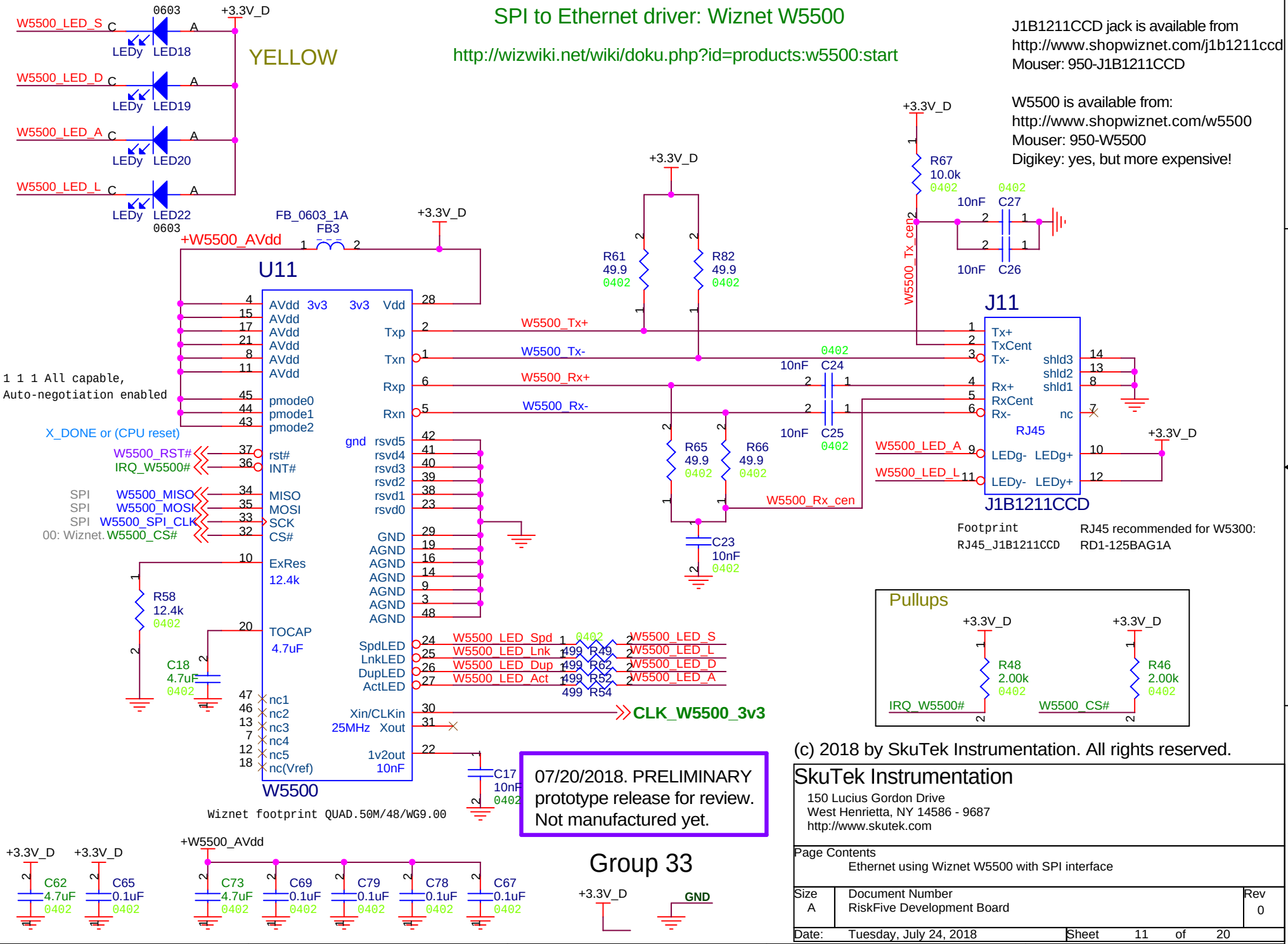
SPI to Ethernet driver: Wiznet W5500

http://wizwiki.net/wiki/doku.php?id=products:w5500:start

J1B1211CCD jack is available from
http://www.shopwiznet.com/j1b1211ccd
Mouser: 950-J1B1211CCD

W5500 is available from:
http://www.shopwiznet.com/w5500
Mouser: 950-W5500
Digikey: yes, but more expensive!



07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.

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Page Contents
Ethernet using Wiznet W5500 with SPI interface

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Ethernet controller and PHY, 16-bit interface

J1B1211CCD jack is available from
http://www.shopwiznet.com/j1b1211ccd
Mouser: 950-J1B1211CCD

W5300 is available from:
http://www.shopwiznet.com/w5300
Mouser: 950-W5300
Digikey: $8.48/ea, more expensive!

U10

W5300

LQFP100 (14x14)

34 pins

From Reset Generator
X_DONE or (pwr down)
W5300_RST#

W5300 must be externally reset after power up.

W5300_D[15:0]
W5300_A[9:1]

ADDR0 is ignored in 16-bit mode.

W5300_WR#
W5300_RD#
W5300_CS#
IRQ_W5300#
W5300_brdy[3:0]
Buffer Ready Indicator

+W5300_3a3
+3.3V_D
+W5300_1a8
+W5300_1.8V_D
+W5300_1v8_out

12.3k 1% RSET_BG

R44 12.4k 0402

TXOP / TXON
RXIP / RXIN
/FDX
/LINKLED
/SPDLED(MII_TXD0)
/FDXLED(MII_TXD1)
/COLLED(MII_TXD2)
/RXLED(MII_TXD3)
/TXLED(MII_TXEN)
MII_TXC
MII_RXC
MII_RXDV
MII_RXD0
MII_RXD1
MII_RXD2
MII_RXD3
MII_COL
MII_CRS

W5300_Tx+
W5300_Tx-
W5300_Rx+
W5300_Rx-

R39 499 W5300_LINK_LED
R40 499 W5300_SPD_LED
R41 499 W5300_FDX_LED
R36 499 W5300_Rx_LED
R37 499 W5300_Tx_LED

OP_MODE0
OP_MODE1
OP_MODE2
NC
NC
NC
NC

000 : Auto-negotiation enable with all capabilities
OPMODE

Ext PHY only OSC25_in
R81 49.9

CLK_W5300_1v8

XTLP
XTLN

TEST_MODE0
TEST_MODE1
TEST_MODE2
TEST_MODE3

0000 : Internal PHY.

Digiparts footprint: VQFP-100_XILINX

R59 2.00k 0402
IRQ_W5300#

C29 0.1uF 0402
C76 0.1uF 0402
C28 0.1uF 0402
R71 49.9 0402
R70 49.9 0402
R69 49.9 0402
R68 49.9 0402

J12
J1B1211CCD
Footprint
RJ45_J1B1211CCD
RD1-125BAG1A

Tx+ TxCent Tx- Rx+ RxCent Rx-
shld3 shld2 shld1 nc
RJ45
LEDg- LEDg+ LEDy- LEDy+

W5300_LINK_LED
W5300_ACT_LED

DS1
R38 2.00k 0402
W5300_Tx_LED
W5300_Rx_LED
W5300_ACT_LED
BAT54AW-7-F
SOT-323_3PADS

BAT54AW-7-F Diodes
Schottky pair SC-70

Group 34

C64 4.7uF 0402
C77 0.1uF 0402
C63 0.1uF 0402
C75 0.1uF 0402
C56 0.1uF 0402
C57 0.1uF 0402
C61 0.1uF 0402
C54 4.7uF 0402
C55 0.1uF 0402
C58 0.1uF 0402
FB_0603_1A FB2

C50 4.7uF 0402
C49 0.1uF 0402
C66 0.1uF 0402
C53 0.1uF 0402
C68 0.1uF 0402
C52 4.7uF 0402
C59 0.1uF 0402
FB_0603_1A FB1

W5300_LINK_LED LED14 0603 YELLOW
W5300_SPD_LED LED15 0603
W5300_FDX_LED LED16 0603
W5300_Rx_LED LED12 0603
W5300_Tx_LED LED13 0603

07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Derived from W5300 Internal PHY reference schematic

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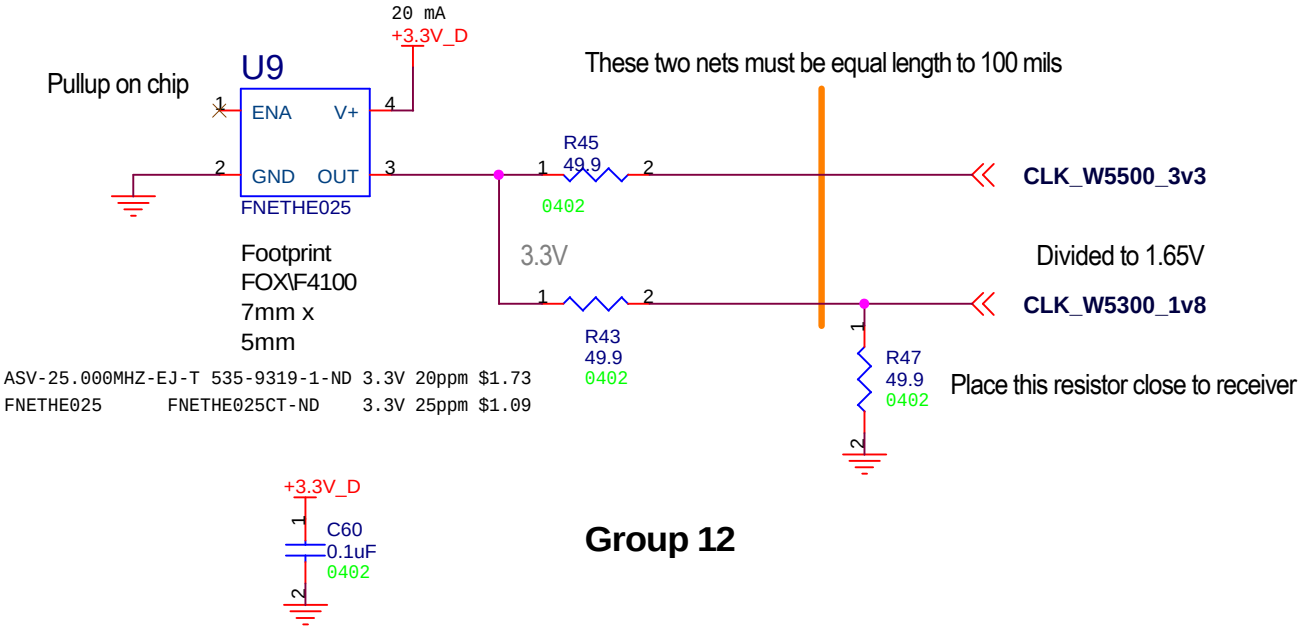
Page Contents: Ethernet using Wiznet W5300

Size: Custom | Document Number: RiskFive Abone Development Board | Rev: 0

Date: Tuesday, July 24, 2018 | Sheet 12 of 20

Clock driver 25 MHz CMOS 3.3V and 1.8V

This clock is driving the Ethernet chips. In order to avoid a fan-out buffer I am using two source-terminated nets. Additionally, the W5300 clock is reduced down to 1.74V (close enough to 1.8V).



Group 12

07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.

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Page Contents	Ethernet clock driver	
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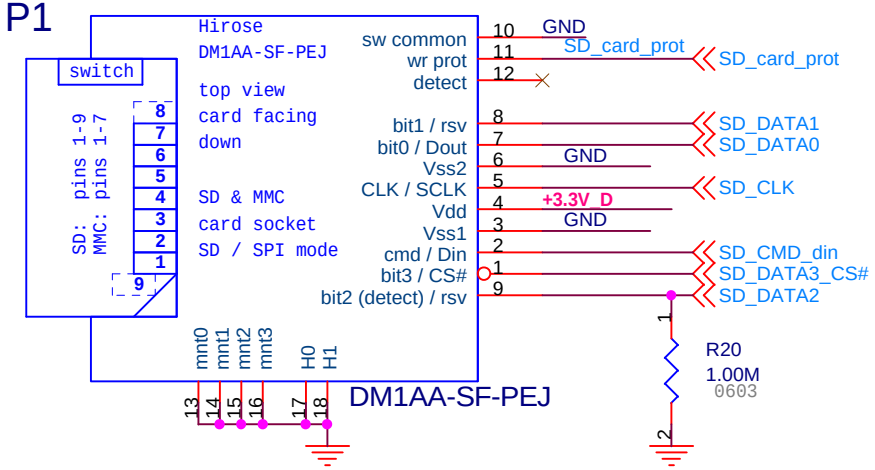
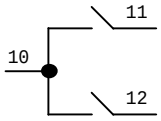
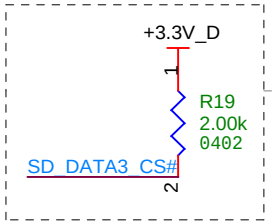
SD / MMC full size card socket

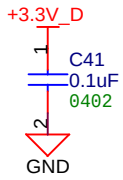
Socket SD/MMC HRS DM1AA-SF-PEJ Still available on Dec/18/2017

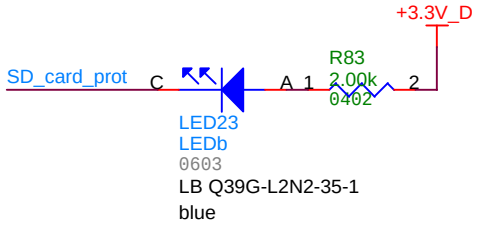




Bit2 (detect) has on-card pullup 50k used to detect the SD card. A large pulldown is needed here.







A visual indication of the SD card protection switch. This could not be routed to theFPGA due to shortage of Hirose pins. Visual warning is the 2nd best. The LED should be red, but I am using blue to avoid introducing yet another part number.

Notes

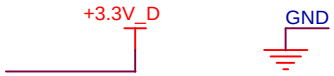
Compgroup 2 is used for initial placement.

The card detection scheme seems different from the one employed with the uSD card, while in fact they should be the same. It needs be reviewed.

The physical "protect switch" will detect the position of the "write protect" switch on the SD card. MMC card does not have that switch. Pullups are needed.

DM1AA-SF-PEJ - SD Memory Card Connectors - Hirose Electric
DigiKey HR845CT-ND $4.67

Card detect not implemented due to shortage of Hirose pins



07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.

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Page Contents: SD card sockets

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PS2 connectors

http://www.burtonsys.com/PS2_keyboard_and_mouse_mini-DIN-6_connector_pinouts.html
http://pinouts.ru/InputCables/Ps2KeyboardYThinkpad.shtml
http://pinouts.ru/Inputs/KeyboardPC6_pinout.shtml

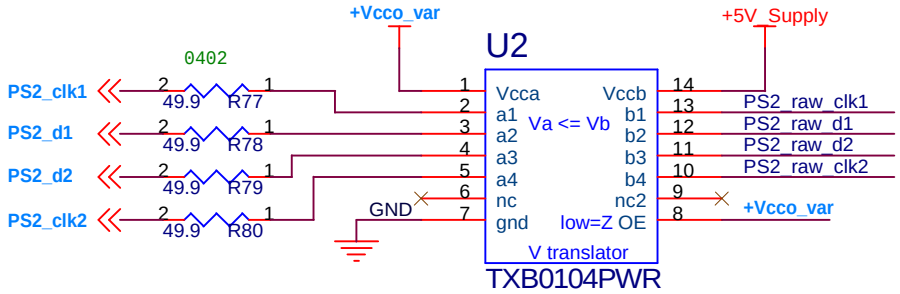
Alternatively, this connector can be used as GPIO with 5V levels.

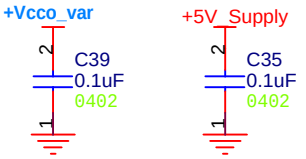
PS2 connector is 6-pin Mini DIN
Footprint in the DIN library
DINC/MIN_TM/6 is REVERSED
Fixed in Digiparts.LLB

Mouse and Keyboard

Use low driving current and serial termination at the FPGA side.

TXS0104 has OC outputs with 4k pullup on chip.
TXB0104 has push-pull outputs.
OE active HIGH (!) is referenced to Vcca.





07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Mouse / keyboard Vcc = 5V
FPGA only tolerates 4V

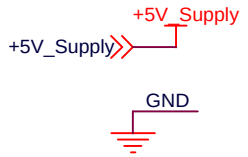
http://pinouts.ru/InputCables/Ps2KeyboardYThinkpad.shtml

Con	signal	Keybrd	Mouse
1	dat1	----	1 (data)
2	dat2	1 (data)	----
3	gnd	3 (gnd)	3 (gnd)
4	Vcc	4 (Vcc)	4 (Vcc)
5	clk1	----	5 (clk)
6	clk2	5 (clk)	----

http://www.computer-engineering.org/ps2protocol/
Summary: Power Specifications
Vcc = +4.5V to +5.5V.
Max Current = 275 mA.

Voltage trans 4bit TXB0104PWR
SOG.65M/14/WG6.50/L5.0

Group 25



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Page Contents
Logic IO for PS2 or general purpose 5V logic IO

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VGA DAC driver

ADV7125BCPZ170
48LFCSP

U14 ADV7125BCPZ170

VGA_red[0:7]
VGA_grn[0:7]
VGA_blue[0:7]

VGA_red0 41 red0 R0
VGA_red1 42 red1
VGA_red2 43 red2
VGA_red3 44 red3
VGA_red4 45 red4
VGA_red5 46 red5
VGA_red6 47 red6
VGA_red7 48 red7 R7
VGA_grn0 3 grn0 G0
VGA_grn1 4 grn1
VGA_grn2 5 grn2
VGA_grn3 6 grn3
VGA_grn4 7 grn4
VGA_grn5 8 grn5
VGA_grn6 9 grn6
VGA_grn7 10 grn7 G7
VGA_blue0 16 blue0 B0
VGA_blue1 17 blue1
VGA_blue2 18 blue2
VGA_blue3 19 blue3
VGA_blue4 20 blue4
VGA_blue5 21 blue5
VGA_blue6 22 blue6
VGA_blue7 23 blue7 B7

RED
GRN
BLUE

VGA_sync# 12 sync#
VGA_blank# 11 blank#
VGA_pix_clk 24 PCLK

1 gnd1
2 gnd2
14 gnd3
15 gnd4
25 gnd5
26 gnd6
39 gnd7
40 gnd8

49 v1
50 v2
51 v3

v4 v5 v6 v7 v8 v9 v10 v11 v12 v13
52 53 54 55 56 57 58 59 60 61

34 outR → MON_RED → R73 75 0603 → GND
33 outR# → GND
32 outG → MON_GRN → R74 75 0603 → GND
31 outG# → GND
28 outB → MON_BLUE → R75 75 0603 → GND
27 outB# → GND

37 Rset → R63 560 0402 → GND
560 ohm PwrSave#
38 PwrSave# → +3.3V_D
35 Comp → C84 0.1uF 0402
0.1uF
36 VREF → C85 0.1uF 0402
1.235V
13 Vaa1
3.3V or 5V 29 Vaa2 → VGA_Vaa
30 Vaa3

62 v16
63 v15
64 v14

Tot = 24+3+2+2= 31
RGB: 24
CTRL: 3
I2C: 2
HVsync: 2

J14A

MON_RED 1 red
MON_GRN 2 green
MON_BLUE 3 blue
4 id2 (res)
GND 5 gnd
VGA
VGA_female_RA

"res" = reserved, do not use

VGA female socket
ICD15S13E6GX00LF
AHDF15A-KG-TAXB
VGA_DSUB_HD_15PINS
or DSUBHD/RS/TM/15

J14B

6 mnt1 Hole1
7 r_rtn
8 g_rtn
9 b_rtn
10 +5V
gnd
VGA mnt2 Hole2
VGA_female_RA

+5V_Supply
R57 12.4k 0402
R53 12.4k 0402

J14C

MON_SDA 11 id0
MON_HSYNC 12 id1 / SDA
MON_VSYNC 13 Hsync
MON_SCL 14 Vsync
15 id3 / SCL
VGA
VGA_female_RA

VGA_shield

U12

+3.3V_D → Vcc_DDC
Vcc (+5V) ← +5V_Supply
ena
MON_RED → vid1
MON_GRN → vid2
MON_BLUE → vid3
out = monitor
in = controller
byp → MON_BYP 0.22uF needed
VGA_SDA → DDC_in1 → DDC_out1 → MON_SDA
VGA_VSYNC → sync_in1 → sync_out1 → MON_VSYNC
VGA_HSYNC → sync_in2 → sync_out2 → MON_HSYNC
VGA_SCL → DDC_in2 → DDC_out2 → MON_SCL
gnd
CM2006-02QR

CM2006-02QR
ESD protection

C22 1nF/250V 1206

R64 1.00M 0603
R60 1.00M

VGA_Vaa C72 0.1uF 0402
VGA_Vaa C83 0.1uF 0402
+3.3V_D C74 0.1uF 0402
+5V_Supply C80 0.1uF 0402
MON_BYP C70 0.1uF 0402
C71 0.1uF 0402

07/20/2018. PRELIMINARY
prototype release for review.
Not manufactured yet.

+3.3V_D
VGA_Vaa

It does not want to connect +5V_Supply accross the pages.
+5V_Supply
GND

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VGA video DAC with ESD protection

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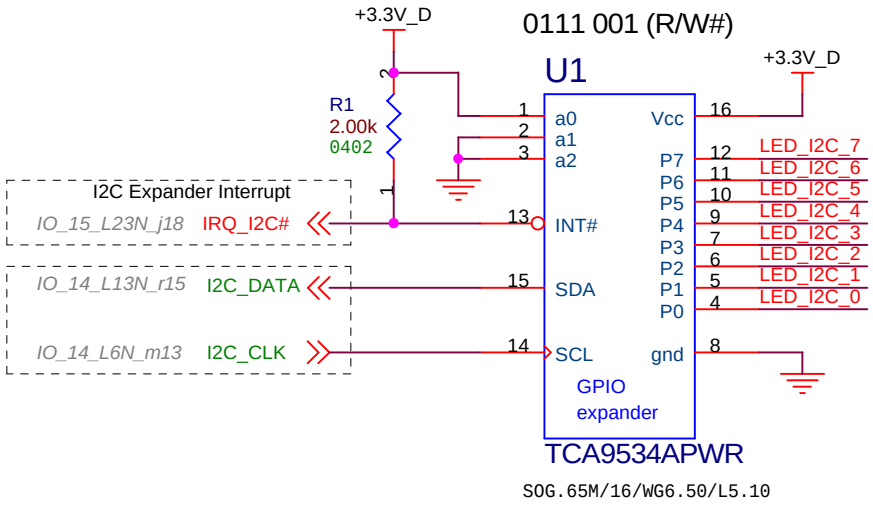
I2C Expander and diagnostic LEDs, active LOW

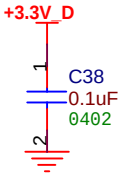
There were not enough pins to connect the LEDs directly to the FPGA

Expander slave address 0111 a2 a1 a0 (R/W#)
Push-pull output structure on P0..P7.
Max freq 400 kHz

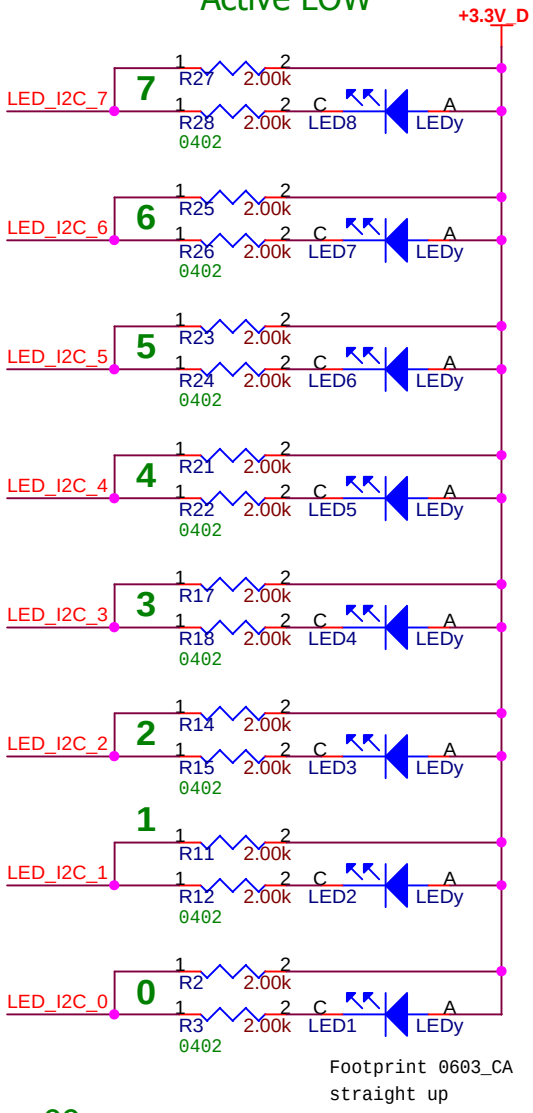


LED signals can be used as chip select pins. The pullups provide a well defined HIGH default.

LED_I2C_[0:7]
LED and/or chip select

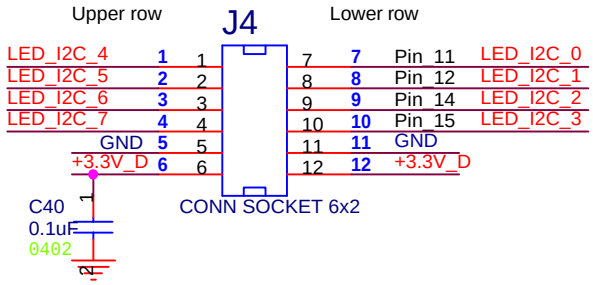


Status LED's Active LOW



Footprint 0603_CA
straight up

PMOD with slow GPIO



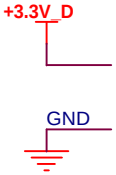
0603 up

LTST-C190TGKT	grn bright
LTST-C190KGKT	grn dim
LTST-C190KSKT	yellow
LTST-C190KFKT	orange
LTST-C190KRKT	red
LTST-C190KAKT	red
LTST-C190TBKT	blue

0402 up

APHHS1005CGCK	grn	40 mcd
APHHS1005SYCK	yllw	150 mcd
APHHS1005SECK	orng	150 mcd
APHHS1005SURCK	red	70 mcd
APHHS1005QBC/D	blue	60 mcd

07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.



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Diagnostic LEDs

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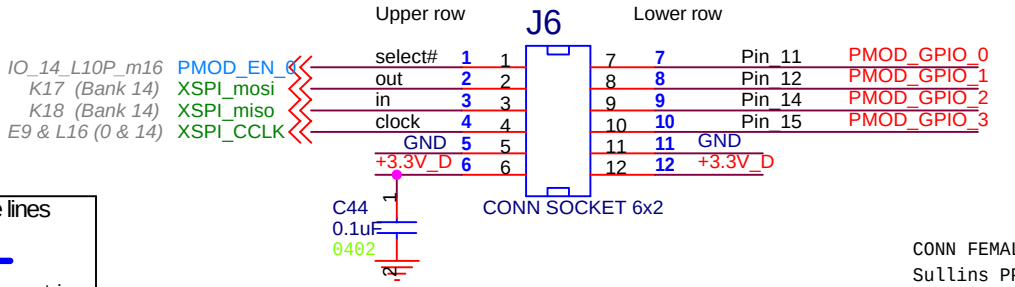
PMOD connector with SPI and FPGA GPIO

According to Digilent Pmod Interface Specification dated November 20, 2011

Upper row of the Pmod Interface Type 2 (SPI) is the same as the Digilent JTAG Cable III pinout. The lower row is not well specified in the Digilent document. Several of their PMODs utilize GPIOs on the lower row. For example, the lower row implements interrupt pins in several PMODs.

Note non-standard pin numbering (in bold) of 12-pin headers.

SPI PMOD #0 with fast GPIO



PMOD Enable lines

PMOD_EN_[0:1]

RTS/CTS are alternative

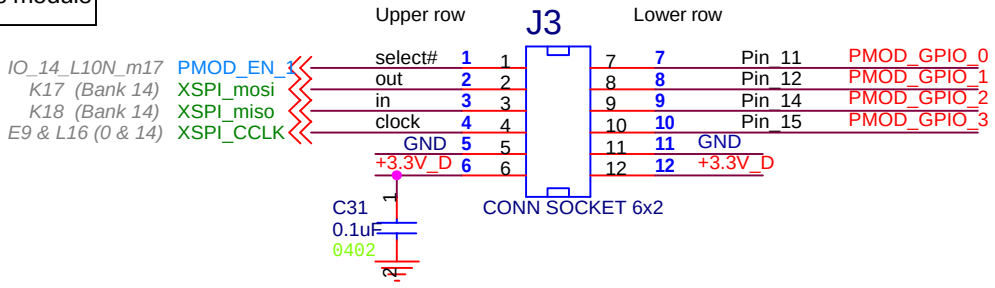
Fast PMOD

S.Hirose PMOD_GPIO_[0:3]

Also used for wireless module

CONN FEMALE 12POSDL .1" R/A GOLD
Sullins PPPC062LJBN-RC
DigiKey S5559-ND

SPI PMOD #1 with fast GPIO



07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.

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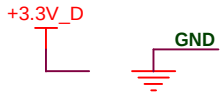

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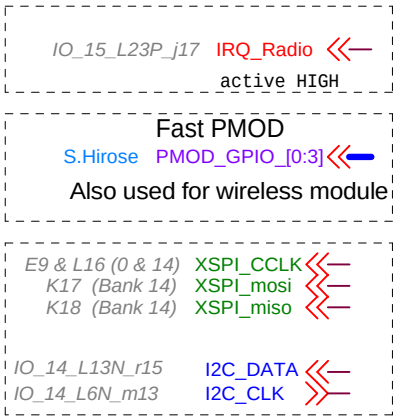
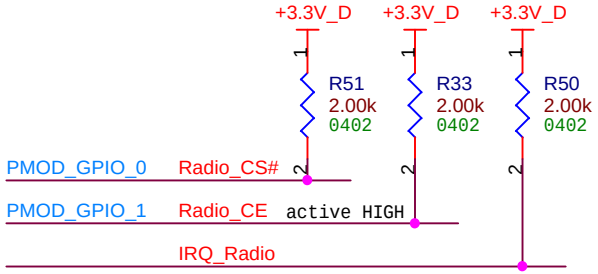
SPI & I2C connector for wireless or other uses

Possible SPI peripherals:
1) NRF24L01 module
2) Anything else.

The socket pinout is compatible with the NRF24L01 wireless module which was used in 2013 FPGA Oberon. Any other SPI application is possible as well. I2C pins were added for completness.

http://www.nordicsemi.com/eng/Products/2.4GHz-RF/nRF24L01P
Nordic Semiconductor
nRF24L01P_Product_Specification_1_0.pdf; Page 50.
See also:
http://randomnerdtutorials.com/nrf24l01-2-4ghz-rf-transceiver-module-with-arduino/
https://gadgetperfect.wordpress.com/nrf24l001-rf-module2-4ghzinterfacing/





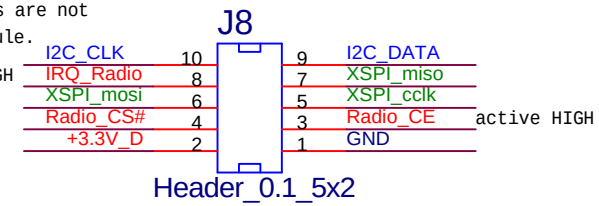
NRF24L01 module, top view

Wire loop antenna

I2C is extra. These two pins are not present in the NRF24L01 module.

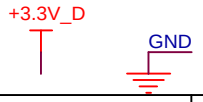
active HIGH

CE is active HIGH
CS# is SPI signal



Amphenol 67997-210HLF (gold)
Amphenol 67997-410HLF (tin)

07/20/2018. PRELIMINARY prototype release for review. Not manufactured yet.



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