Artix FPGA On Module (FOM)

REV	Description	DATE	BY
0	01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.	01/10/2018	ws
0.1	01/16/2018. Added wireless socket to the Abone. Not manufactured yet.	01/16/2018	ws

01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

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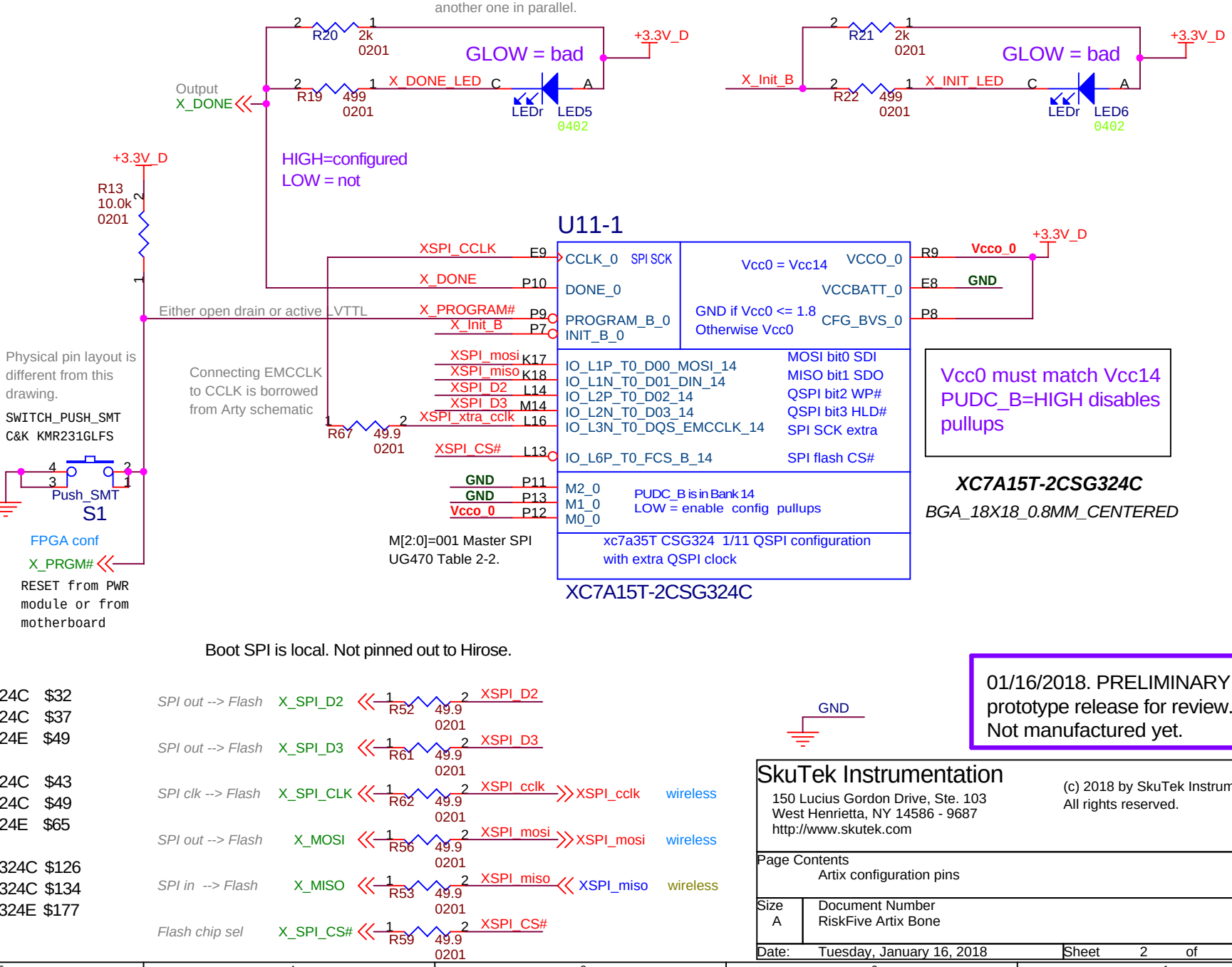
Artix configuration pins

```
APHHS1005CGCK   grn   40 mcd
APHHS1005SYCK   yllw 150 mcd
APHHS1005SECK   orng 150 mcd
APHHS1005SURCK  red   70 mcd
APHHS1005QBC/D  blue  60 mcd
```

LED is not a good pullup, so we need another one in parallel.



Boot SPI is local. Not pinned out to Hirose.

XC7A15T-1CSG324C	$32
XC7A15T-2CSG324C	$37
XC7A15T-3CSG324E	$49
XC7A35T-1CSG324C	$43
XC7A35T-2CSG324C	$49
XC7A35T-3CSG324E	$65
XC7A100T-1CSG324C	$126
XC7A100T-2CSG324C	$134
XC7A100T-3CSG324E	$177

GND

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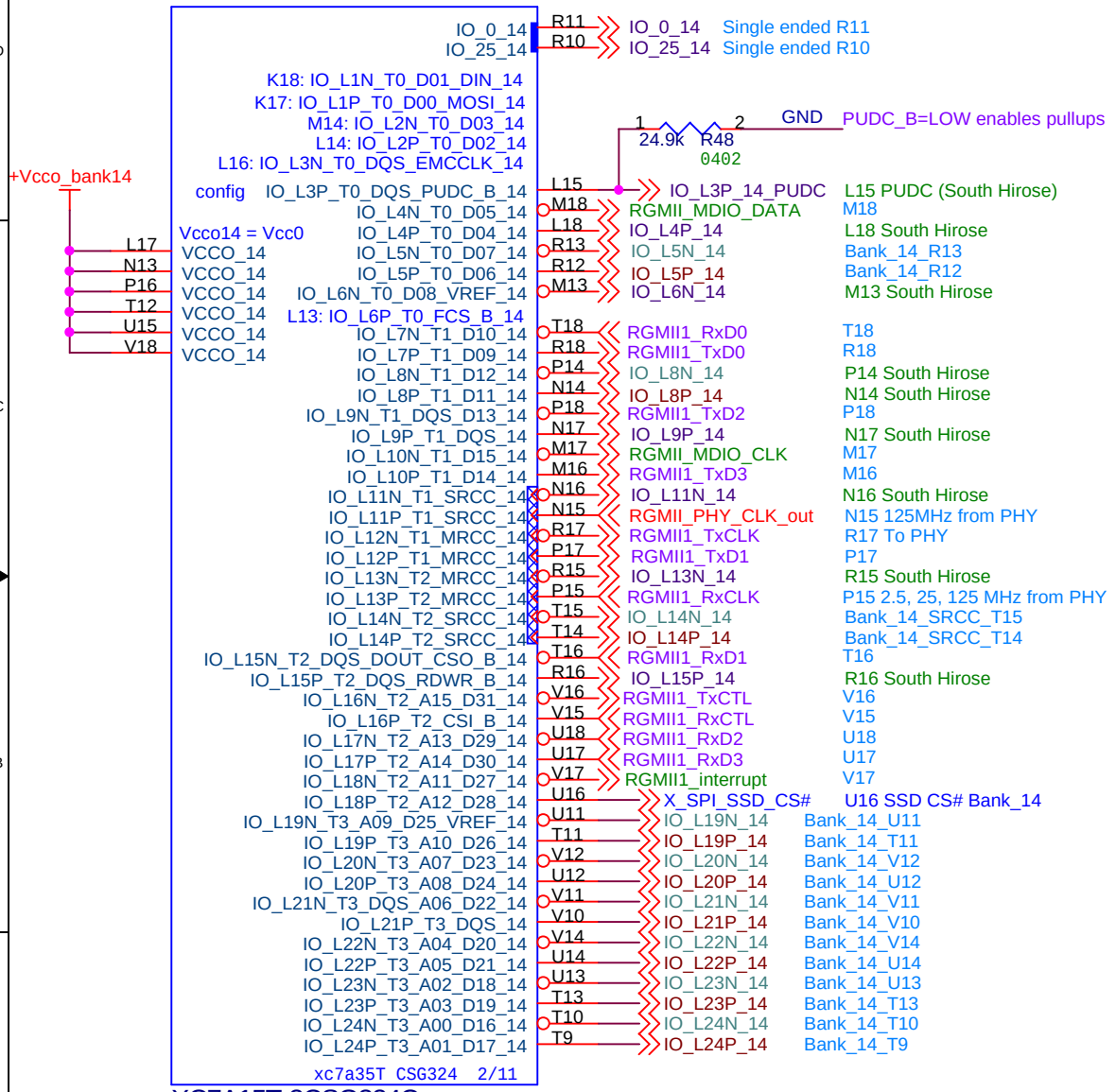
Artix Bank 14

50 I/O per bank

Must be the same as Bank 0.
Use the same Vcc as flash.

This bank contains some configuration pins.

U11-2



XC7A15T-2CSG324C

+Vcco_bank14

L17, N13, P16, T12, U15, V18

R11 IO_0_14 Single ended R11
R10 IO_25_14 Single ended R10

1 24.9k R48 2 0402 GND PUDC_B=LOW enables pullups

L15	IO_L3P_14_PUDC	L15 PUDC (South Hirose)
M18	RGMII_MDIO_DATA	M18
L18	IO_L4P_14	L18 South Hirose
R13	IO_L5N_14	Bank_14_R13
R12	IO_L5P_14	Bank_14_R12
M13	IO_L6N_14	M13 South Hirose
T18	RGMII1_RxD0	T18
R18	RGMII1_TxD0	R18
P14	IO_L8N_14	P14 South Hirose
N14	IO_L8P_14	N14 South Hirose
P18	RGMII1_TxD2	P18
N17	IO_L9P_14	N17 South Hirose
M17	RGMII_MDIO_CLK	M17
M16	RGMII1_TxD3	M16
N16	IO_L11N_14	N16 South Hirose
N15	RGMII_PHY_CLK_out	N15 125MHz from PHY
R17	RGMII1_TxCLK	R17 To PHY
P17	RGMII1_TxD1	P17
R15	IO_L13N_14	R15 South Hirose
P15	RGMII1_RxCLK	P15 2.5, 25, 125 MHz from PHY
T15	IO_L14N_14	Bank_14_SRCC_T15
T14	IO_L14P_14	Bank_14_SRCC_T14
T16	RGMII1_RxD1	T16
R16	IO_L15P_14	R16 South Hirose
V16	RGMII1_TxCTL	V16
V15	RGMII1_RxCTL	V15
U18	RGMII1_RxD2	U18
U17	RGMII1_RxD3	U17
V17	RGMII1_interrupt	V17
U16	X_SPI_SSD_CS#	U16 SSD CS# Bank_14
U11	IO_L19N_14	Bank_14_U11
T11	IO_L19P_14	Bank_14_T11
V12	IO_L20N_14	Bank_14_V12
U12	IO_L20P_14	Bank_14_U12
V11	IO_L21N_14	Bank_14_V11
V10	IO_L21P_14	Bank_14_V10
V14	IO_L22N_14	Bank_14_V14
U14	IO_L22P_14	Bank_14_U14
U13	IO_L23N_14	Bank_14_U13
T13	IO_L23P_14	Bank_14_T13
T10	IO_L24N_14	Bank_14_T10
T9	IO_L24P_14	Bank_14_T9

+3.3V_D +Vcco_bank14

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XC7A15T-2CSG324C

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Artix Bank 34

Video and North Hirose. All video signals except audio and I2C are also connected to Hirose.

50 I/O per bank

Video=28 wires
RGMII=16 wires

LVDS requires 2.5V

+3.3V_D +Vcco_bank34

+Vcco_bank34

3.3V

U11-5

K4 VCCO_34
N3 VCCO_34
P6 VCCO_34
T2 VCCO_34
U5 VCCO_34
V8 VCCO_34
1.2V-3.3V

IO_0_34	K6	I2C0_SCL	K6 TDA and MAC EEPROM; local
IO_25_34	U8	IO_25_34	U8 (Bank34)
IO_L1N_T0_34	M1	TDA_red7	M1 Red7_LCD_15
IO_L1P_T0_34	L1	TDA_SYNC_V	L1 TDA V_sync
IO_L2N_T0_34	L3	TDA_SYNC_H	L3 TDA H_sync
IO_L2P_T0_34	K3	TDA_interrupt	K3 TDA interrupt
IO_L3N_T0_DQS_34	N1	TDA_red1	N1 Red1
IO_L3P_T0_DQS_34	N2	TDA_red0	N2 Red0
IO_L4N_T0_34	M2	TDA_red6	M2 Red6_LCD_14
IO_L4P_T0_34	M3	TDA_red5	M3 Red5_LCD_13
IO_L5N_T0_34	L4	TDA_audio_CLK	L4 I2S audio clk
IO_L5P_T0_34	K5	I2C0_SDA	K5 TDA and MAC EEPROM
IO_L6N_T0_VREF_34	L5	TDA_audio_frame	L5 Audio frame (word sel)
IO_L6P_T0_34	L6	TDA_audio_0	L6 I2S stream 0 (local)
IO_L7N_T1_34	V1	IO_L7N_34	V1 (Bank34) North
IO_L7P_T1_34	U1	TDA_blue4	U1 Blue4_LCD_1
IO_L8N_T1_34	U3	TDA_blue6	U3 Blue6_LCD_3
IO_L8P_T1_34	U4	TDA_blue7	U4 Blue7_LCD_4
IO_L9N_T1_DQS_34	V2	IO_L9N_34	V2 (Bank34) North
IO_L9P_T1_DQS_34	U2	TDA_blue5	U2 Blue5_LCD_2
IO_L10N_T1_34	V4	IO_L10N_34	V4 (Bank34) North
IO_L10P_T1_34	V5	IO_L10P_34	V5 (Bank34) North
IO_L11N_T1_SRCC_34	T3	TDA_blue2	T3 Blue2; srcc-
IO_L11P_T1_SRCC_34	R3	TDA_blue0	R3 Blue0; srcc+
IO_L12N_T1_MRCC_34	T4	IO_L12N_MRCC	T4 (Bank34) mrcc-
IO_L12P_T1_MRCC_34	T5	IO_L12P_MRCC	T5 (Bank34); mrcc+
IO_L13N_T2_MRCC_34	P5	TDA_gr4	P5 Green4_LCD_7; mrcc-
IO_L13P_T2_MRCC_34	N5	**CLK_SYS_bank34**	**N5 System clk 100 MHz**
IO_L14N_T2_SRCC_34	P3	TDA_gr6	P3 Green6_LCD_9; srcc-
IO_L14P_T2_SRCC_34	P4	TDA_gr5	P4 Green5_LCD_8; srcc+
IO_L15N_T2_DQS_34	R2	TDA_gr2	R2 Green2_LCD_5
IO_L15P_T2_DQS_34	P2	TDA_gr7	P2 Green7_LCD_10
IO_L16N_T2_34	N4	TDA_red2	N4 Red2
IO_L16P_T2_34	M4	TDA_PCLK	M4 TDA Video Pixel_clk
IO_L17N_T2_34	T1	TDA_blue1	T1 Blue1
IO_L17P_T2_34	R1	TDA_gr3	R1 Green3_LCD_6
IO_L18N_T2_34	N6	TDA_red4	N6 Red4_LCD_12
IO_L18P_T2_34	M6	TDA_DE	M6 TDA Video Data Enable
IO_L19N_T3_VREF_34	R5	TDA_gr1	R5 Green1
IO_L19P_T3_34	R6	TDA_gr0	R6 Green0
IO_L20N_T3_34	V6	IO_L20N_34	V6 (Bank34) North
IO_L20P_T3_34	V7	IO_L20P_34	V7 (Bank34) North
IO_L21N_T3_DQS_34	V9	IO_L21N_34	V9 (Bank34) North
IO_L21P_T3_DQS_34	U9	IO_L21P_34	U9 (Bank34) North
IO_L22N_T3_34	U6	IO_L22N_34	U6 (Bank34) North
IO_L22P_T3_34	U7	IO_L22P_34	U7 (Bank34) North
IO_L23N_T3_34	T6	TDA_blue3	T6 Blue3_LCD_0
IO_L23P_T3_34	R7	TDA_red3	R7 Red3_LCD_11
IO_L24N_T3_34	T8	IO_L24N_34	T8 (Bank34) North
IO_L24P_T3_34	R8	IO_L24P_34	R8 (Bank34) North

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XC7A15T-2CSG324C

XC7A15T-2CSG324C

BGA_18X18_0.8MM_CENTERED

GND

MAC ID

TDA and FPGA Bank34
I2C0_SCL
I2C0_SDA
TDA and FPGA Bank34

Pullups are on HDMI page

U1

SCL 1
SDA 3
VCC 4
VSS 2
WP 5

+3.3V_D

C36
0.1uF
0201

24AA02E48T-I/OT

WP pin is n.c. in this part

MAC ID EPPROM on I2C0
Plastic SOT-23, 5-lead
Address = 1010 000

01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

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Artix DDR3 Bank 35

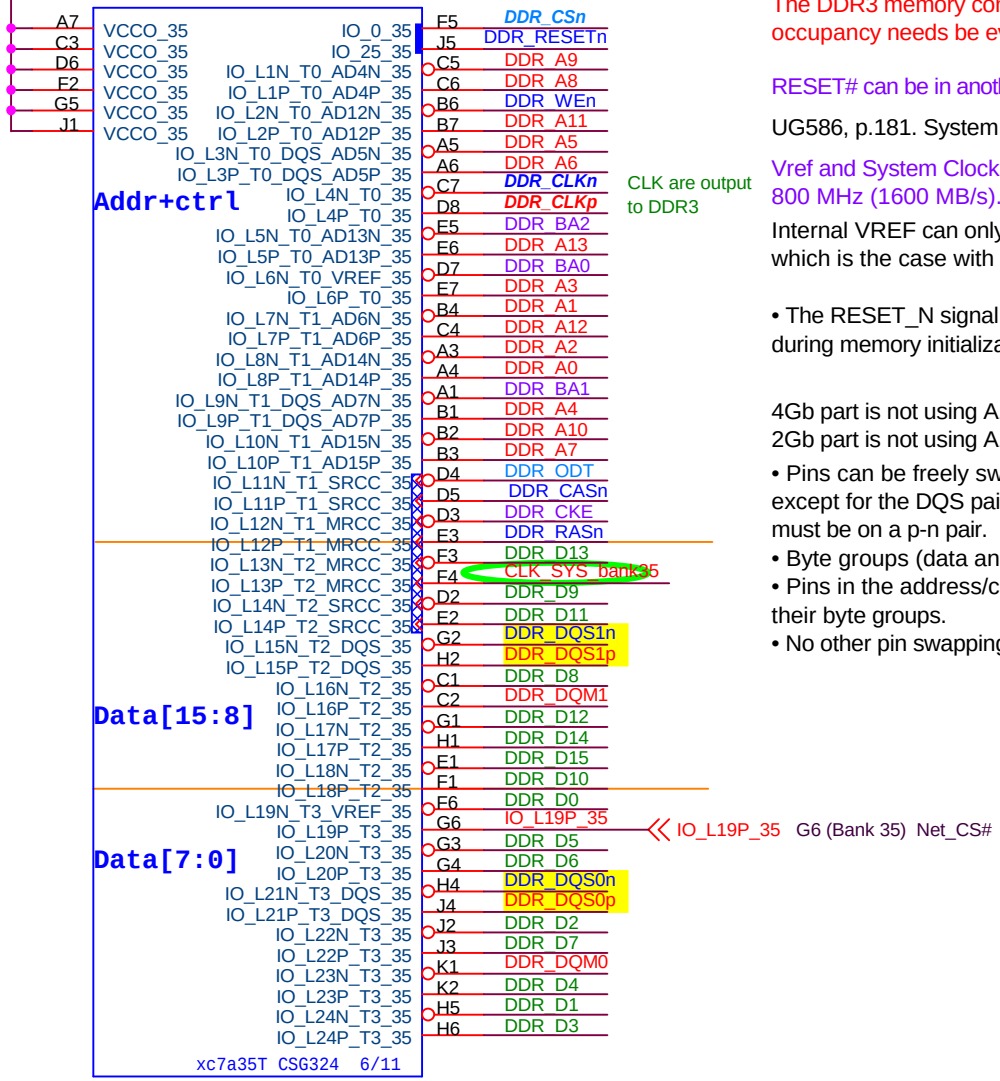
50 I/O per bank

1.35V or 1.50V **1.5V**

+Vdds_DDR

DDR_CSN can be on IO_0 because
Addresses are on adjacent group T0;
AND CK is output from T0

U11-6



XC7A15T-2CSG324C

CLK are output to DDR3

IO_L19P_35 G6 (Bank 35) Net_CS#

The memory controller firmware can be similar to Open Cores
http://opencores.org/project,wb2axip

The DDR3 memory controller takes about 9k flip-flops. The impact on the FPGA occupancy needs be evaluated before committing the board to production.

RESET# can be in another Bank!

UG586, p.181. System Clock must be in the same column. It means Bank 34 or 35.

Vref and System Clock are the optimizations to reach the high data rate up to 800 MHz (1600 MB/s). Artix cannot do it anyway. Vref is not necessary.

Internal VREF can only be used for data rates of 800 Mb/s or below, which is the case with Artix.

• The RESET_N signal is not terminated. This signal should be pulled down during memory initialization with a 4.7 kohm resistor connected to GND.

4Gb part is not using A15 in x16 mode. It only uses [14:0].
2Gb part is not using A14 in x16 mode. It only uses [13:0].

• Pins can be freely swapped within each byte group (data and address/control), except for the DQS pair which must be on a clock-capable DQS pair and the CK which must be on a p-n pair.
• Byte groups (data and address/control) can be freely swapped with each other.
• Pins in the address/control byte groups can be freely swapped within and between their byte groups.
• No other pin swapping is permitted.

CLK_SYS_bank16 System clk to bank 16
CLK_SYS_bank34 System clk to bank 34
CLK_SYS_bank35 System clk to bank 35
DDR_D[15..0]
DDR_BA[2..0]
DDR_A[15..0] Input
DDR_CSn
DDR_CLKp Output
DDR_CLKn Output
DDR_ODT
DDR_CASn
DDR_RASn
DDR_WEn
DDR_CKE
DDR_DQS1p
DDR_DQS1n
DDR_DQS0p
DDR_DQS0n
DDR_RESETn
DDR_DQM0 UDM
DDR_DQM1 LDM
DQM0 with DQS0
DQM1 with DQS1

01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

GND

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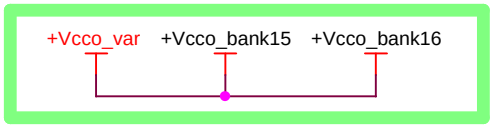

Artix Banks 15 and 16

These banks do not contain configuration pins.

60 pins in total

+Vcco_bank15

LVDS requires using 2.5V

U11-3

A17	VCCO_15	Vcc0 = Vcc15	IO_0_15	G13	IO_0_15 G13 (Bank 15, SE)
C13	VCCO_15		IO_25_15	K16	IO_25_15 K16 (Bank 15, SE)
D16	VCCO_15		IO_L1N_T0_AD0N_15	C14	IO_L1N_15 C14 (Bank 15)
G15	VCCO_15		IO_L1P_T0_AD0P_15	D14	IO_L1P_15 D14 (Bank 15)
H18	VCCO_15		IO_L2N_T0_AD8N_15	B14	IO_L2N_15 B14 (Bank 15)
K14	VCCO_15		IO_L2P_T0_AD8P_15	B13	IO_L2P_15 B13 (Bank 15)
			IO_L3N_T0_DQS_AD1N_15	B12	IO_L3N_15 B12 (Bank 15)
			IO_L3P_T0_DQS_AD1P_15	C12	IO_L3P_15 C12 (Bank 15)
			IO_L4N_T0_15	A11	IO_L4N_15 A11 (Bank 15)
			IO_L4P_T0_15	B11	IO_L4P_15 B11 (Bank 15)
			IO_L5N_T0_AD9N_15	F14	IO_L5N_15 F14 (Bank 15)
			IO_L5P_T0_AD9P_15	F13	IO_L5P_15 F13 (Bank 15)
			IO_L6N_T0_VREF_15	D13	IO_L6N_15 D13 (Bank 15)
			IO_L6P_T0_15	D12	IO_L6P_15 D12 (Bank 15)
			IO_L7N_T1_AD2N_15	B17	IO_L7N_15 B17 (Bank 15)
			IO_L7P_T1_AD2P_15	B16	IO_L7P_15 B16 (Bank 15)
			IO_L8N_T1_AD10N_15	A16	IO_L8N_15 A16 (Bank 15)
			IO_L8P_T1_AD10P_15	A15	IO_L8P_15 A15 (Bank 15)
			IO_L9N_T1_DQS_AD3N_15	A14	IO_L9N_15 A14 (Bank 15)
			IO_L9P_T1_DQS_AD3P_15	A13	IO_L9P_15 A13 (Bank 15)
			IO_L10N_T1_AD11N_15	A18	IO_L10N_15 A18 (Bank 15)
			IO_L10P_T1_AD11P_15	B18	IO_L10P_15 B18 (Bank 15)
			IO_L11N_T1_SRCC_15	E16	IO_L11N_15 E16 (Bank 15) srcc
			IO_L11P_T1_SRCC_15	E15	IO_L11P_15 E15 (Bank 15) srcc
			IO_L12N_T1_MRCC_15	C15	IO_L12N_15 C15 (Bank 15) mrcc
			IO_L12P_T1_MRCC_15	D15	IO_L12P_15 D15 (Bank 15) mrcc
			IO_L13N_T2_MRCC_15	G16	IO_L13N_15 G16 (Bank 15) mrcc
			IO_L13P_T2_MRCC_15	H16	IO_L13P_15 H15 (Bank 15) mrcc
			IO_L14N_T2_SRCC_15	F16	IO_L14N_15 F16 (Bank 15) srcc
			IO_L14P_T2_SRCC_15	F15	IO_L14P_15 F15 (Bank 15) srcc
			IO_L15N_T2_DQS_ADV_B_15	G14	IO_L15N_15 G14 (Bank 15)
			IO_L15P_T2_DQS_15	H14	IO_L15P_15 H14 (Bank 15)
			IO_L16N_T2_A27_15	D17	IO_L16N_15 D17 (Bank 15)
			IO_L16P_T2_A28_15	E17	IO_L16P_15 E17 (Bank 15)
			IO_L17N_T2_A25_15	J13	IO_L17N_15 J13 (Bank 15)
			IO_L17P_T2_A26_15	K13	IO_L17P_15 K13 (Bank 15)
			IO_L18N_T2_A23_15	G17	IO_L18N_15 G17 (Bank 15)
			IO_L18P_T2_A24_15	H17	IO_L18P_15 H17 (Bank 15)
			IO_L19N_T3_A21_VREF_15	H15	IO_L19N_15 H15 (Bank 15)
			IO_L19P_T3_A22_15	J14	IO_L19P_15 J14 (Bank 15)
			IO_L20N_T3_A19_15	C17	IO_L20N_15 C17 (Bank 15)
			IO_L20P_T3_A20_15	C16	IO_L20P_15 C16 (Bank 15)
			IO_L21N_T3_DQS_A18_15	D18	IO_L21N_15 D18 (Bank 15)
			IO_L21P_T3_DQS_15	E18	IO_L21P_15 E18 (Bank 15)
			IO_L22N_T3_A16_15	F18	IO_L22N_15 F18 (Bank 15)
			IO_L22P_T3_A17_15	G18	IO_L22P_15 G18 (Bank 15)
			IO_L23N_T3_FWE_B_15	J18	IO_L23N_15 J18 (Bank 15)
			IO_L23P_T3_FOE_B_15	J17	IO_L23P_15 J17 (Bank 15)
			IO_L24N_T3_RS0_15	J15	IO_L24N_15 J15 (Bank 15)
			IO_L24P_T3_RS1_15	K15	IO_L24P_15 K15 (Bank 15)

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+Vcco_bank16

U11-4

B10

VCCO_16	IO_L6N_T0_VREF_16	D9	IO_L6N_16 D9 (Bank 16)
	IO_L11N_T1_SRCC_16	B9	IO_L11N_16 B9 (Bank 16) srcc
	IO_L11P_T1_SRCC_16	C9	IO_L11P_16 C9 (Bank 16) srcc
	IO_L12N_T1_MRCC_16	A8	IO_L12N_16 A8 (Bank 16) mrcc-
	IO_L12P_T1_MRCC_16	B8	CLK_SYS_bank16 B8 (Bank 16) mrcc+
	IO_L13N_T2_MRCC_16	C10	IO_L13N_16 C10 (Bank 16) mrcc
	IO_L13P_T2_MRCC_16	C11	IO_L13P_16 C11 (Bank 16) mrcc
	IO_L14N_T2_SRCC_16	A9	IO_L14N_16 A9 (Bank 16) srcc S.Hirose
	IO_L14P_T2_SRCC_16	A10	IO_L14P_16 A10 (Bank 16) srcc
	IO_L19N_T3_VREF_16	D10	IO_L19N_16 D10 (Bank 16) N.Hirose

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XC7A15T-2CSG324C

UART

```
D18 Tx
D12 Rx
D13 RTS#
D14 CTS#
C14 extra
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01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

XC7A15T-2CSG324C

BGA_18X18_0.8MM_CENTERED

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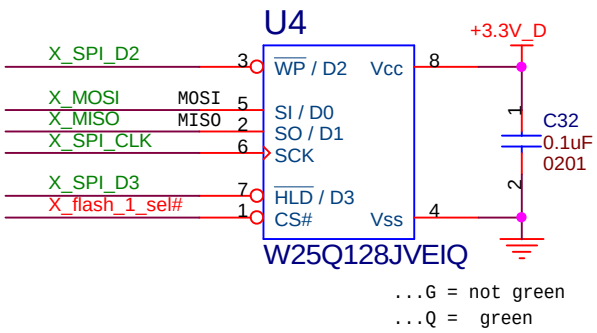
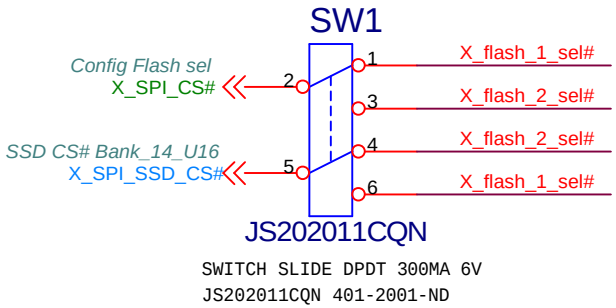
Artix configuration SPI flash and Solid State Disk

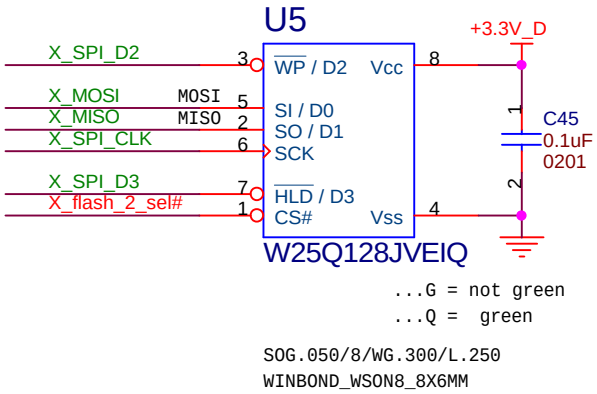
Two possible use cases:
1) Dual boot.
2) Boot and SSD.

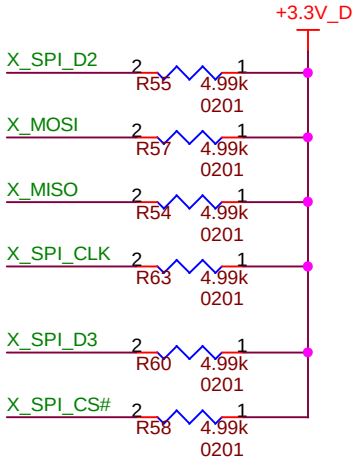
SPI CLK is the same pin as Configuration CCLK. It can be used after configuration via STARTUP2 "primitive" described in UG470 v1.8 page 94. On this board I also routed pin L16 (L6P_EMCCLK) to the same CCLK. The "primitive" is not necessary.





Compatible 8x6 parts
SO-8 W25Q128JVSI
WSON W25Q128JVEI





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GND

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Page Contents
SPI configuration flash

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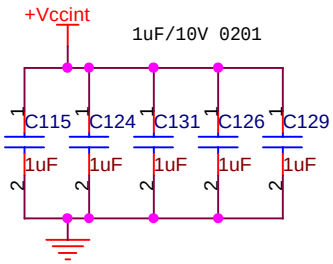
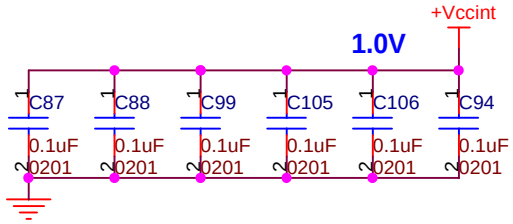
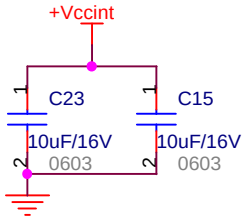
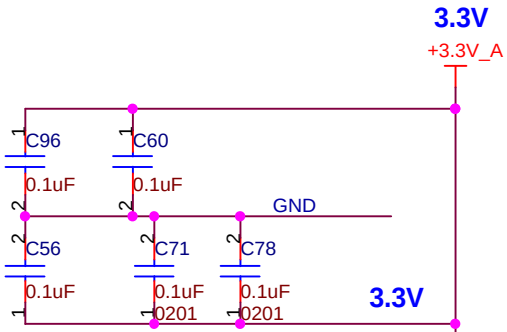
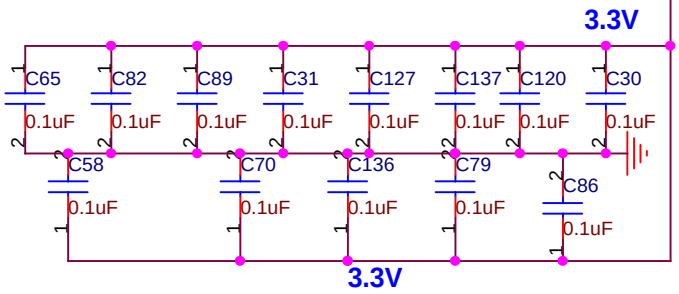
FPGA power filtering

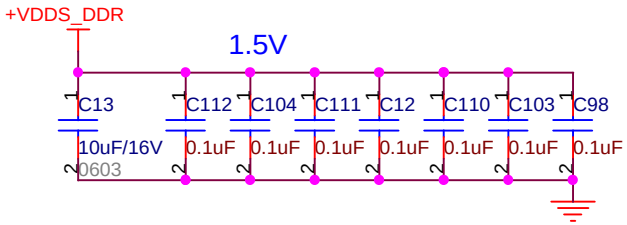


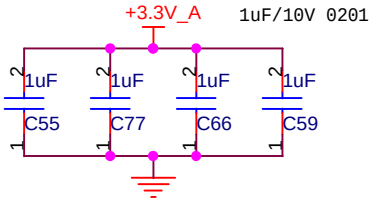


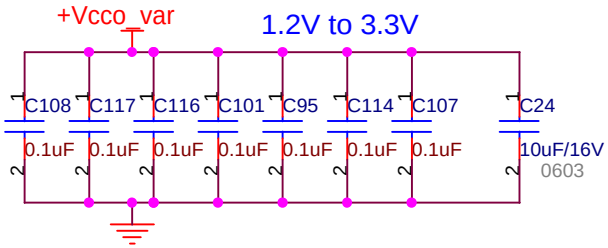












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FPGA decoupling

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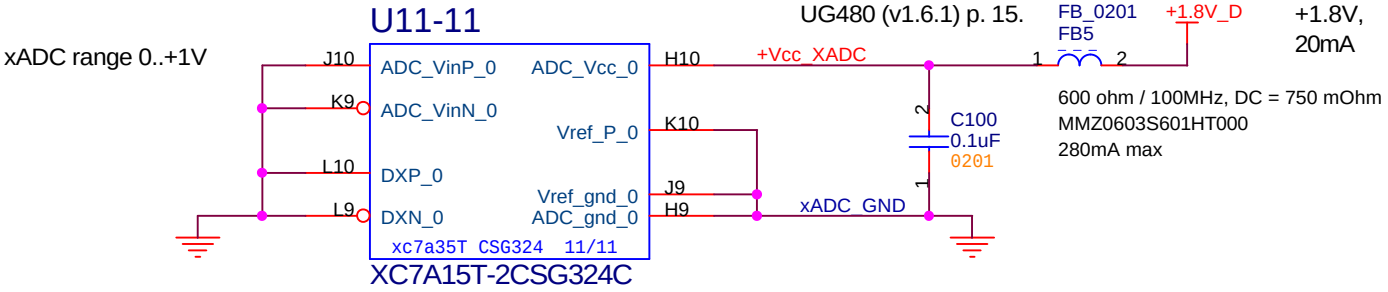
Artix xADC

Powering and using xADC: see UG480 (v1.6.1) p. 77.

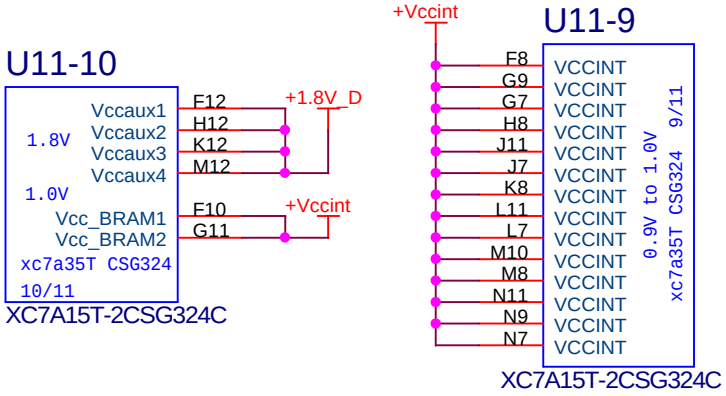
P.14: xADC internal schematics and on-die sensors.
P.15: How to connect xADC pins.

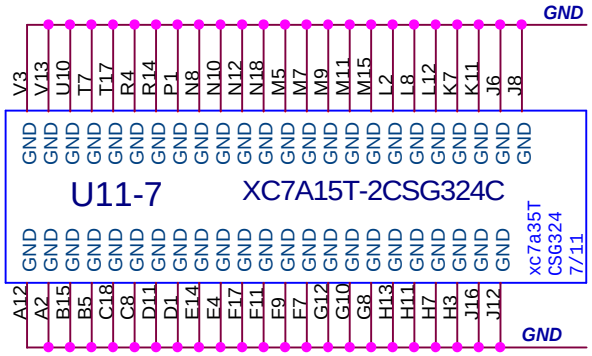


XC7A15T-2CSG324C

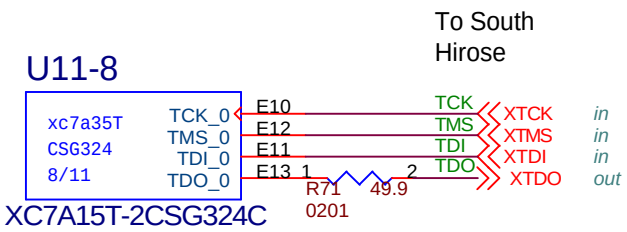
BGA_18X18_0.8MM_CENTERED

Artix GND, VccAUX, VccBRAM, and Vccint





Artix JTAG



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Page Contents: Artix JTAG, xADC, GND, VccAUX, VccBRAM, and Vccint

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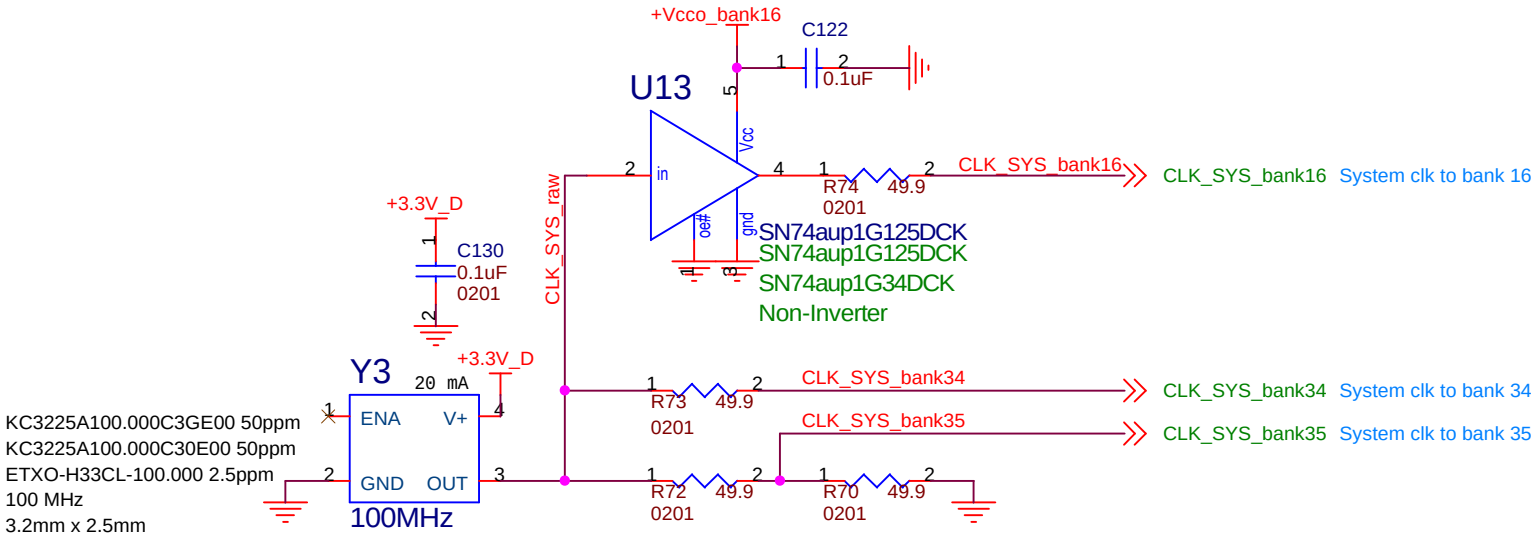
System clock 100 MHz



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Page Contents
System clock 100 MHz

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DDR3 memory design with Artix-7

ug586_7Series_MIS.PDF V 2.0 (2014)

P.181: DDR3 SDRAM. This section describes guidelines for DDR3 SDRAM designs, including bank selection, pin allocation, pin assignments, termination, I/O standards, and trace lengths.

Four DQS byte groups are available in each 50-pin bank. Each byte group consists of a clock-capable I/O pair for the DQS and 10 associated I/Os.

Several times in this document byte groups are referenced for address and control as well, this refers to the 12 associated groups. In a typical DDR3 data bus configuration, eight of these 10 I/Os are used for the DQs, one is used for the data mask (DM), and one is left over for other signals in the memory interface.

• The system clock input must be in the same column as the memory interface. The system clock input is recommended to be in the address/control bank, when possible.

• CK must be connected to a p-n pair in one of the control byte groups. Any p-n pair in the group is acceptable, including SRCC, MRCC, and DQS pins.

• DQS signals for a byte group must be connected to a designated DQS pair in the bank due to the dedicated strobe connections for DDR2 and DDR3 SDRAM. For more information, see 7 Series FPGAs Clocking Resources User Guide (UG472) [Ref 9].

• DQ and DM (if used) signals must be connected to the byte group pins associated with the corresponding DQS.

• The non-byte groups pins (that is, top/bottom most pins in HR banks ["single-ended", I think] can be used for an address/control pin, if the following conditions are met:

° The adjacent byte group (T0/T3) is used as an address/control byte group.

° An unused pin exists in the adjacent byte group (T0/T3) or the CK output is contained in the adjacent byte group.

• Control (RAS_N, CAS_N, WE_N, CS_N, CKE, ODT) and address lines must be connected to byte groups not used for the data byte groups.

• RESET_N can be connected to any available pin within the device, as long as timing is met and an appropriate I/O voltage standard is used. The GUI restricts this pin to the banks used for the interface to help with timing, but this is not a requirement.

Voltage reference Vref

Internal VREF can only be used for data rates of 800 Mb/s or below.

External VREF must track the midpoint of the VDD supplied to the DRAM and ground, done with resistive divider. VREF traces need to have a larger than the minimum spacing to reduce coupling from other intrusive signals.

Termination

Termination resistors are not needed because the memory chip has on-die termination (ODT) on data lines. Address lines are not terminated. From Micron Data Sheet:

On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16. ... ODT is referenced to VREFCA.

DDR3 Layout CLK DQS Skew https://forums.xilinx.com/xlnx/board/crawl_message?board.id=MIG&message.id=9618

The specified delay (skew) range is only taking into account package and board-level delays. Anything within the FPGA is already factored in to these numbers. CLK phase does not change. It runs continuously. DQS is used by the FPGA as a training pattern to determine the internal relationship between the continuous clock and the received data edges. 150ps to 1600ps of delay represents the range which the calibration circuitry can compensate for.

CK/CK# signals must arrive at each memory device after the DQS/DQS# signals. The skew allowed between CK/CK# and DQS/DQS# must be bounded between 0 and 1,600 ps. The recommended skew between CK/CK# and DQS/DQS# is 150 ps to 1,600 ps for components / UDIMMs and for RDIMMs it is 450 ps to 750 ps.

Page 183. Pin Swapping.

• Pins can be freely swapped within each byte group (data and address/control), except for the DQS pair which must be on a clock-capable DQS pair and the CK which must be on a p-n pair.

• Byte groups (data and address/control) can be freely swapped with each other.

• Pins in the address/control byte groups can be freely swapped within and between their byte groups.

• No other pin swapping is permitted.

Page 183. System Clock, PLL and MMCM Locations, and Constraints.

The PLL and MMCM are required to be in the bank that supplies the clock to the memory. The system clock input is also strongly recommended to be in this bank. The exception is a 16-bit interface in a single bank where there might not be pins available for the clock input. In this case, the clock input needs to come from an adjacent bank through the frequency backbone to the PLL. The system clock input to the PLL must come from clock capable I/O.

The system clock input can only be used for an interface in the same column.

Unused outputs from the PLL can be used as clock outputs. Only the settings for these outputs can be changed. Settings related to the overall PLL behavior and the used outputs must not be disturbed.

A PLL cannot be shared among interfaces. See Clocking Architecture, page 109 for information on allowed PLL parameters.

VCCAUX_IO

VCCAUX_IO has two values that can be set to 1.8V or 2.0V depending on memory performance. VCCAUX_IO might need to be its own supply that can be adjusted. For performance information, see the 7 Series FPGAs Data Sheets [Ref 12]. For more information on VCCAUX_IO, see 7 Series SelectIO™ Resources User Guide (UG471) [Ref 1], “VCCAUX_IO” section.

Which FPGA device?

The DDR3 memory controller takes about 9k flip-flops. The impact on the design occupancy needs be evaluated before committing the board to production. The smallest 15T device may be too small to fit the memory controller, CPU, video controller, and other logic.

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DDR3 Design with Artix-7

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2Gb DDR3

U10 DDR3L SDRAM

4Gb part is not using A15 in x16 mode. It only uses [14:0].
2Gb part is not using A14 in x16 mode. It only uses [13:0].

On-Die Termination (ODT) is not provided on chip.

On-Die Termination (ODT) is provided on chip.

The RESET_N signal is not terminated. This signal should be pulled down during memory initialization with a 4.7 kohm resistor connected to GND.

R25 10.0k 0201

R29 2k.DNP 0201

R28 4.99k 0201

DDR_RESETn

DDR_CLKp, DDR_CLKn, DDR_CKE, DDR_CSn, DDR_RASn, DDR_CASn, DDR_WEn

DDR_D[15..0]

DDR_A[15..0] 3

DDR_BA[2..0] 3,7

DDR_ODT 3,7

DDR_DQS1p, DDR_DQS1n

DDR_DQS0p, DDR_DQS0n

DDR_DQM1, DDR_DQM0

+VDDS_DDR

1.5V or 1.35V

GND

Extra cap

DDR_VREF

C76 0.1uF 0201

C69, C54, C81, C64, C75 0.1uF 0201

C113, C57, C74, C97, C102 0.1uF 0201

C63, C53, C93, C68 0.1uF 0201

R65 4.99k 0201

R66 4.99k 0201

C92 0.1uF 0201

C85 0.1uF 0201

R26 240 0201

AS4C128M16D3L

There are several memory chips starting with AS4C128M16D3L

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Page Contents: DDR3 memory

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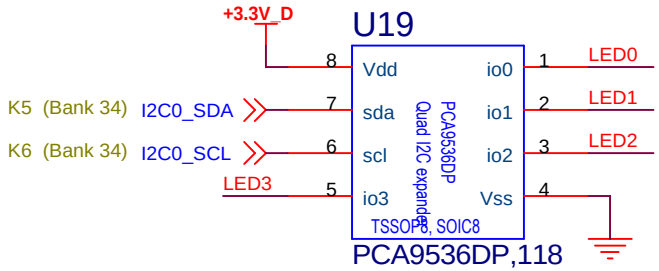
Diagnostic LEDs

There were not enough pins to connect the LEDs directly to the FPGA

```
I2C address bits (Table 1)
H L L L L L H R/W
1 0 0 0 0 0 1 R/W
65 (dec); 0x41 (hex)
```

Quad I2C expander

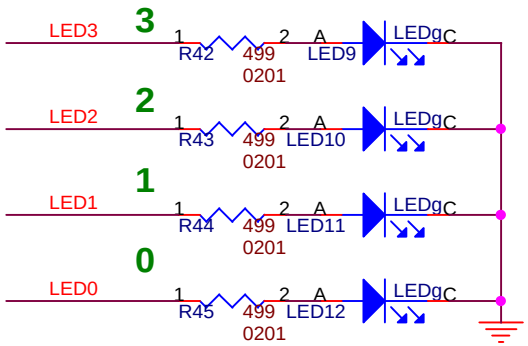


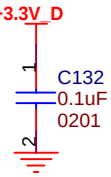
PCA9536DP,118 NXP
PCA9536DGKR TI

SOG.65M/8/WG4.90/L3.00

Status LED's

Footprint 0402_CA
0402 straight up





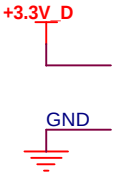
01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

0603 up

LTST-C190TGKT	grn bright
LTST-C190KGKT	grn dim
LTST-C190KSKT	yellow
LTST-C190KFKT	orange
LTST-C190KRKT	red
LTST-C190KAKT	red
LTST-C190TBKT	blue

0402 up

APHHS1005CGCK	grn	40 mcd
APHHS1005SYCK	yllw	150 mcd
APHHS1005SECK	orng	150 mcd
APHHS1005SURCK	red	70 mcd
APHHS1005QBC/D	blue	60 mcd



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Gigabit PHY

RGMII = 16 wires

RGMII rcv clk to MAC	RGMII1_RxCLK	RX_CLK
Rx data 3 to MAC	RGMII1_RxD3	RXD3
Rx data 2	RGMII1_RxD2	RXD2
Rx data 1	RGMII1_RxD1	RXD1
Rx data 0	RGMII1_RxD0	RXD0
RGMII Rx ctrl to MAC	RGMII1_RxCTL	RX_CTRL
RGMII Tx clk from MAC	RGMII1_TxCLK	TxCLK
RGMII tx data 3 from MAC	RGMII1_TxD3	TXD3
RGMII tx data 2	RGMII1_TxD2	TXD2
RGMII tx data 1	RGMII1_TxD1	TXD1
RGMII tx data 0	RGMII1_TxD0	TXD0
RGMII tx enable from MAC	RGMII1_TxCTL	TX_EN
Mngmnt data	RGMII_MDIO_DATA	MDIO
Mngmnt clock	RGMII_MDIO_CLK	MDC

3 signals not used for RGMII: COL, CRS, TxCLK

To processor RGMII1_interrupt — RGMII1_interrupt

Interrupt to FPGA

Synch Ethernet recovered clock

125MHz RGMII_PHY_CLK_out — 2 — 49.9 R27 0201 — 1 — CLK_125_raw

+1.8V

PHY is making its own 1.8V to avoid sequencing.

U9D

Avdd_1v8 (13, 48)
Avdd_2v5 (3, 9) ~200 mA +2.5V_D
Either in or NC
3.3V Vddo (19, 30) +3.3V_D
2.5V Vddo (41)
1.8V Vddo +1.0V_PHY
TMS (22) TDI (23) TDO (21) TCK (20) +3.3V_D
DVdd_1v0 (6) PHY_Vdd10
DVdd_1v0 (24, 31, 42) Max 1.155V ~100 mA
DP83867 GbE PHY 4/4
DP83867CSRGZT

U9C DP83867CSRGZT

DP83867 GbE PHY 3/4

LED0 pin strapping
Mode 1 mirror - SGMII -
Mode 2 mirror - SGMII +
Mode 3 mirror + SGMII -
Mode 4 mirror + SGMII +

gnd49 gnd50 gnd51 gnd52 gnd53 gnd54 gnd55 gnd56 gnd57 gnd58 gnd59 gnd60 gnd61
49 50 51 52 53 54 55 56 57 58 59 60 61

TX_CLK = in, 125/25/2.5 MHz ref clock.
Tx_EN = in, Tx control
RxCLK = out 125/25/2.5 MHz ref clk.
Rx_CTRL = out Rx control
RGMII + MDIO = 16 wires

+1.8V_D — C109 0.1uF

Y2 20 mA +1.8V_D
ENA V+ GND OUT
25MHz
3.2mm x 2.5mm
CTX984CT-ND

HIGH = FPGA configured
LOW = not configured

From FPGA X_DONE
CLK_25_18V

U9B

reset (43) xtal_in_1.8V (15) 25 MHz 1.8V xtal_out_1.8V (14)
intrpt_pdwn (44) LED3 or PTP GPIO_0 GPIO_1 (39, 40) Rbias_11.0k (12)
DP83867 GbE PHY 2/4
DP83867CSRGZT

+3.3V_D — R64 2k 0201 — RGMII1_interrupt
PHY_GPIO_0 — Ether_GPIO_0 PTP Start_Frame
PHY_GPIO_1
R69 11.0k 0201

+2.5V

U8

+3.3V_D — Vin (1, 3) en — Vout (5) ~200 mA +2.5V_D
TLV700xx LDO 200mA SOT23 DDC SC70 DCK
gnd (2) nc (4)
C84 1uF 0201
TLV70025DCK

LDO is stable with 0.1uF, but 1uF is recommended.
TLV70028DCKR or -T.

+1.0V

+1.0V_PHY — PHY_Vdd10 — FB4 220/2A — +Vccint

PHY in QFN package requires 1.0V

Power sequence requirements when 1.8V is not provided: NONE.

Mirrored; D.S. page 35
A . D 0 -> 3
B . C 1 -> 2
C . B 2 -> 1
D . A 3 -> 0

U9A QFN-48

RGMII: RXD0 (33) RXD1 (34) RXD2 (35) RXD3 (36) Rx_CLK (32) Rx_CTRL (38) TXD0 (28) TXD1 (27) TXD2 (26) TXD3 (25) TxCLK (29) Tx_EN (37) CLK_125_raw (18)
RX_CLK_out RX_CTRL_out TX_CLK_in TX_CTRL_in CLK125_out
RJ45 terminated 100 ohm: mdi0_p (1) mdi0_n (2) Ether3+ 11 Ether3- 11; mdi1_p (4) mdi1_n (5) Ether2+ 11 Ether2- 11; mdi2_p (7) mdi2_n (8) Ether1+ 11 Ether1- 11; mdi3_p (10) mdi3_n (11) Ether0+ 11 Ether0- 11
LED2 PHY_LED2 (45) Activity Ether_LED1
LED1 PHY_LED1 (46) 1000 link
LED0 PHY_LED0 (47) Link Ether_LED0
MDC (16) MDIO (17)
DP83867 GbE PHY 1/4
DP83867CSRGZT

+3.3V_D — R68 2k 0201 — MDC MDIO

fmax = 25 MHz

Center tap to AVdd not required. Internal on-chip termination provided on Media Dependent Interface (i.e., magnetics).

PTP stamps are on GPIO pins
D.S. Page 88.

Footprint 0402_CA

GND
PHY_LED1 — R14 499 0201 — LEDg A — LED3 C — 0402 straight up
PHY_GPIO_1 — R16 499 0201 — LEDg A — LED4 C — 0402 straight up

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Compgroup 97

Mode	Rhi	Rlo (p.36)
1	open	open
2	10.0k	2.49k
3	5.76k	2.49k
4	2.49k	open

PHY configuration using strap resistors.
Rx_D0, D2: Mode 1 --> addr = 0
Rx_CTRL: Mode 3 --> auto negotiate.
LED0: Mode 1 --> RGMII w/o mirror.
LED0: Mode 3 --> RGMII with mirror.

R23 2.49k 0201 — Rx_CTRL — R24 5.76k 0201 — +3.3V_B — Mode 3
R17 2.49k 0201 P2.49kABCT-ND — PHY_LED0 — R18 5.76k 0201 P5.76kABCT-ND — +3.3V_B — Mode 3

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Page Contents: GbE PHY

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Texas Instruments PHY

In addition to usual PHY duties, the PHY is supposed to:

1. Recover the 125 MHz clock from Synchronous Ethernet.

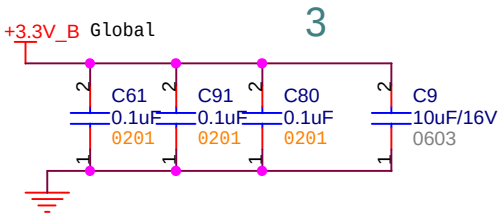
2. Present the 125 MHz clock to the Ethernet MAC.

3. Present this clock to the Hirose connector.

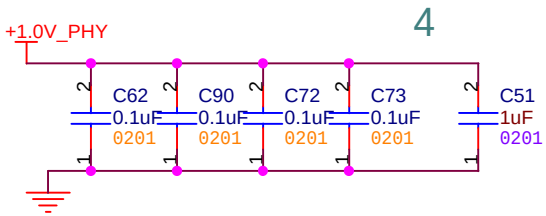
4. Provide PTP services, if we manage to devise the PTP driver. Otherwise the PTP will be ignored. Note that external pulse stamping is not provided by this PHY. Pulse-per-second is not provided, either.

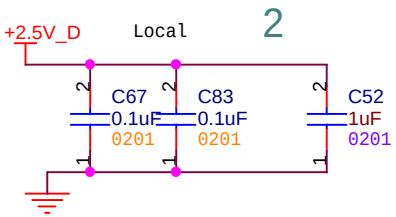
5. The PHY makes its own 1.8V voltage rail w/o decoupling.

6. PHY RGMII is powered with 3.3V to comply with the CPU.



Group 97





01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

0603
10 uF C1608X5R1A106K

0402
10 nF TMK105B7103KV-F
0.1uF C1005X5R1E104K, M
1uF C1005X5R1A105K or M
4.7uF CL05A475MP5NRNC

CAP CER 0.1UF 16V 10% X5R 0201
C0603X5R1C104K030BC TDK

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Page Contents
GbE PHY decoupling

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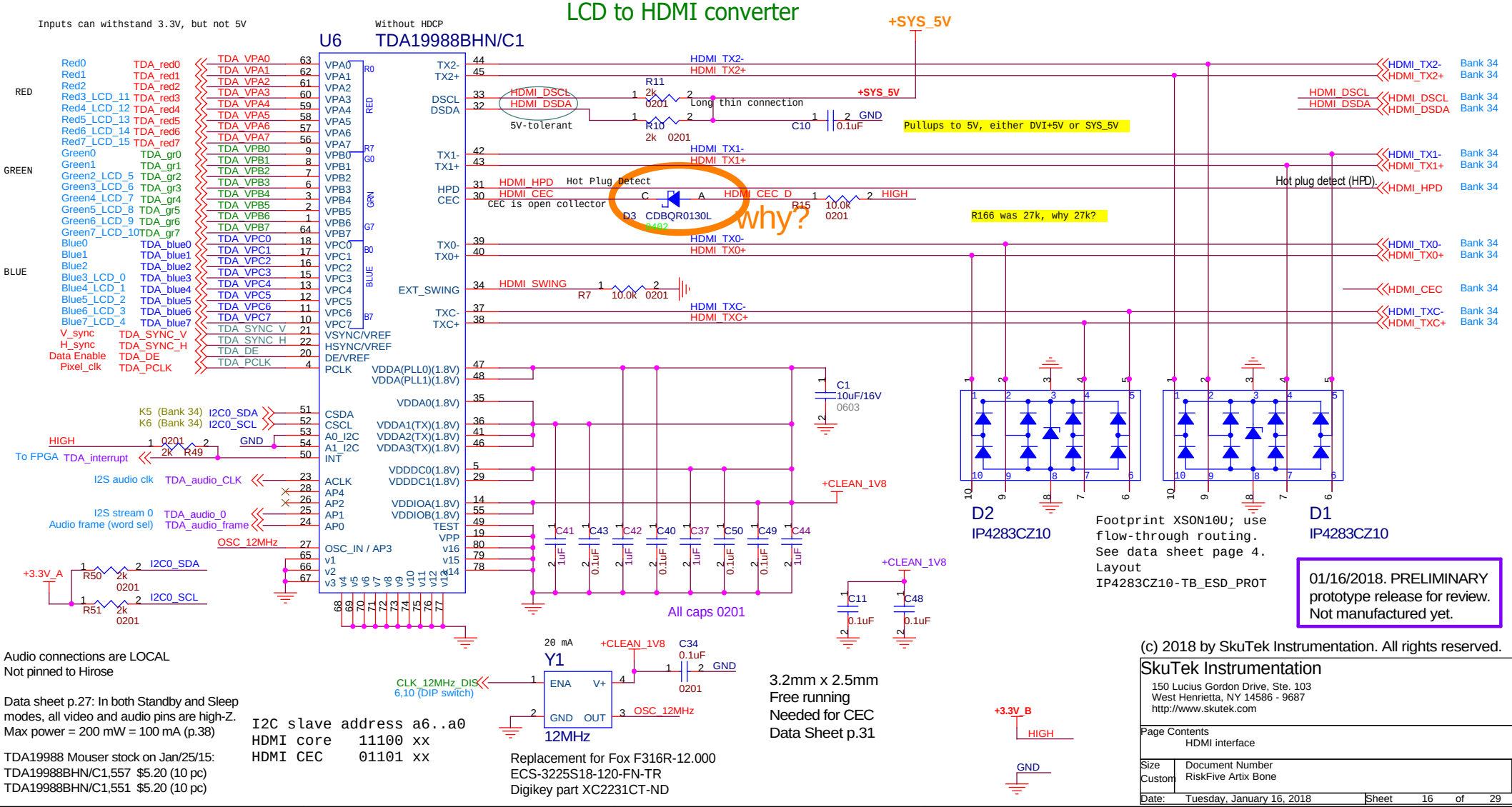
LCD to HDMI converter

Inputs can withstand 3.3V, but not 5V

Without HDCP

U6 TDA19988BHN/C1



Audio connections are LOCAL
Not pinned to Hirose

Data sheet p.27: In both Standby and Sleep modes, all video and audio pins are high-Z.
Max power = 200 mW = 100 mA (p.38)

TDA19988 Mouser stock on Jan/25/15:
TDA19988BHN/C1,557 $5.20 (10 pc)
TDA19988BHN/C1,551 $5.20 (10 pc)

```
I2C slave address a6..a0
HDMI core   11100 xx
HDMI CEC    01101 xx
```

Replacement for Fox F316R-12.000
ECS-3225S18-120-FN-TR
Digikey part XC2231CT-ND

3.2mm x 2.5mm
Free running
Needed for CEC
Data Sheet p.31

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Page Contents: HDMI interface

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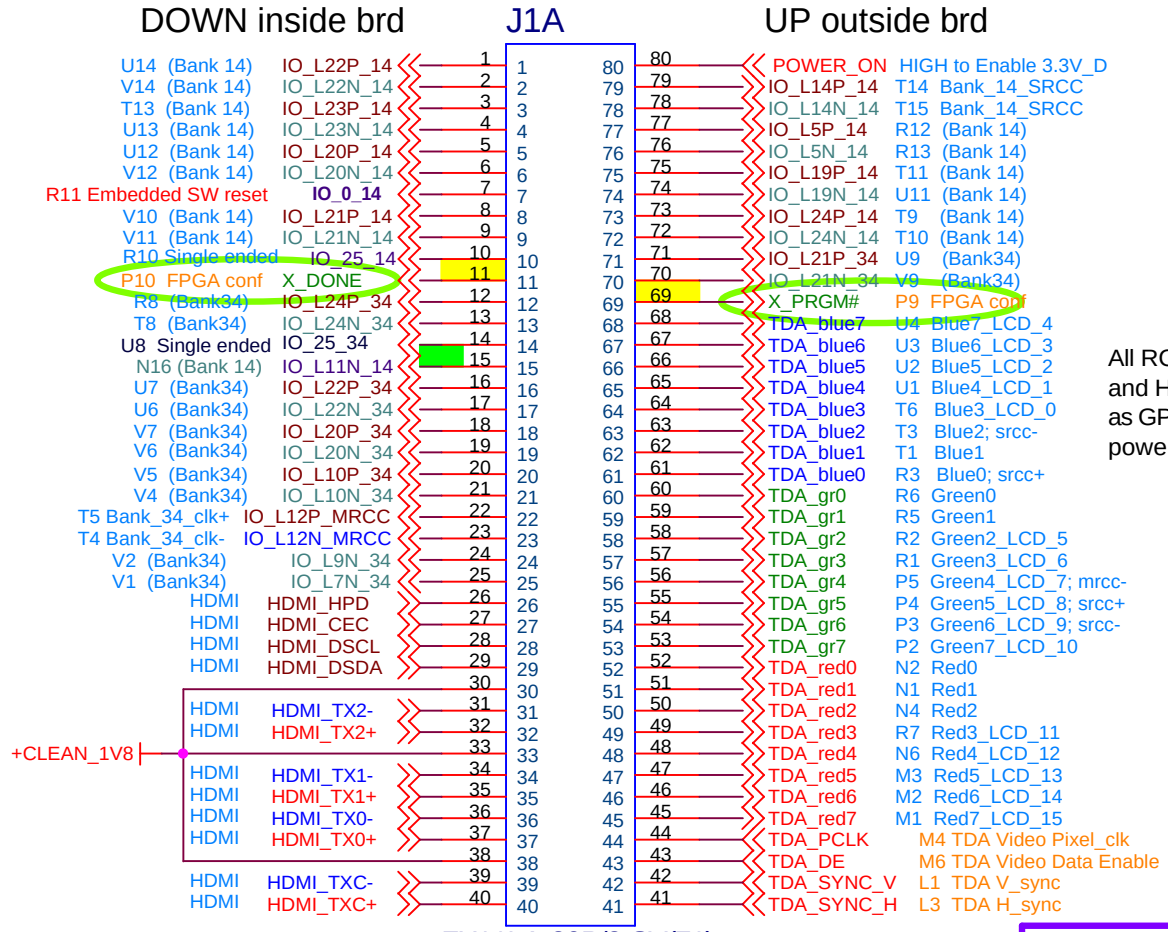
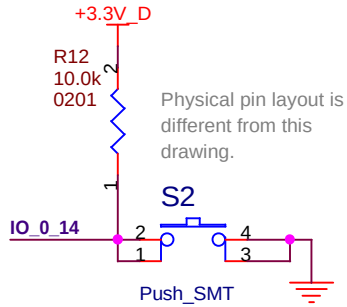
NORTH header



All RGB, pixel clock, V_synch, and H_synch pins can be used as GPIO when the HDMI chip is powered down

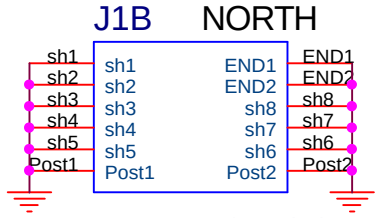
Software reset button. Must be programmed in embedded software. Needs a firmware debouncer.



01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

CONN HEADER 80POS W/POSTS SMD
FX11LA-80P/8-SV(71) -> mezzanine

CONN RECEPT 80POS W/POSTS SMD
FX11LA-80S/8-SV(71) -> motherboard



Footprint FX11L80/H/GP

GND

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Page Contents
High density Hirose connectors

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SOUTH header

FTDI cable with 450mA +5V power
USB --> JTAG, UART
FTDI part C232HD-EDHSP-0

DOWN outside brd

J3A

UP inside brd

		Ether Link	Ether_LED0	1	80	Ether_LED1	Ether activity		
		GbE	Ether2+	2	79	Ether0+	GbE		
		GbE	Ether2-	3	78	Ether0-	GbE		
		GbE	Ether3+	4	77	Ether1+	GbE		
		GbE	Ether3-	5	76	Ether1-	GbE		
		PTP Start_Frame	Ether_GPIO_0	6	75			IO_L8P_14	N14 (Bank 14)
R16 (Bank 14)	IO_L15P_14			7	74			IO_L8N_14	P14 (Bank 14)
R15 (Bank 14)	IO_L13N_14			8	73	Pulldown		IO_L3P_14_PUDC	L15 PUDC
L18 (Bank 14)	IO_L4P_14			9	72			IO_L24P_15	K15 (Bank 15)
M13 (Bank 14)	IO_L6N_14			10	71			IO_L24N_15	J15 (Bank 15)
N17 (Bank 14)	IO_L9P_14			11	70			IO_L18N_15	G17 (Bank 15)
D10 (Bank 16)	IO_L19N_16			12	69			IO_L18P_15	H17 (Bank 15)
K16 (Bank 15, SE)	IO_25_15			13	68			IO_L16N_15	D17 (Bank 15)
J14 (Bank 15)	IO_L19P_15		IO_L19P_15	14	67			IO_L16P_15	E17 (Bank 15)
H15 (Bank 15)	IO_L19N_15		IO_L19n_15	15	66			IO_L20P_15	C16 (Bank 15)
J17 (Bank 15)	IO_L23P_15		IO_L23p_15	16	65			IO_L20N_15	C17 (Bank 15)
J18 (Bank 15)	IO_L23N_15		IO_L23n_15	17	64			IO_L3P_15	C12 (Bank 15)
K13 (Bank 15)	IO_L17P_15		IO_L17p_15	18	63			IO_L3N_15	B12 (Bank 15)
J13 (Bank 15)	IO_L17N_15		IO_L17n_15	19	62			IO_L7P_15	B16 (Bank 15)
H14 (Bank 15)	IO_L15P_15		IO_L15p_15	20	61			IO_L7N_15	B17 (Bank 15)
G14 (Bank 15)	IO_L15N_15		IO_L15n_15	21	60			IO_L10P_15	B18 (Bank 15)
H15 (Bank 15) mrcc	IO_L13P_15		IO_L13p_15	22	59			IO_L10N_15	A18 (Bank 15)
G16 (Bank 15) mrcc	IO_L13N_15		IO_L13n_15	23	58			IO_L2P_15	B13 (Bank 15)
G13 (Bank 15, SE)	IO_0_15		single	24	57			IO_L2N_15	B14 (Bank 15)
G18 (Bank 15)	IO_L22P_15		IO_L22p_15	25	56			IO_L11P_16	C9 (Bank 16) srcc
F18 (Bank 15)	IO_L22N_15		IO_L22n_15	26	55			IO_L11N_16	B9 (Bank 16) srcc
F13 (Bank 15)	IO_L5P_15		IO_L5p_15	27	54			IO_L13P_16	C11 (Bank 16) mrcc
F14 (Bank 15)	IO_L5N_15		IO_L5n_15	28	53			IO_L13N_16	C10 (Bank 16) mrcc
F15 (Bank 15) srcc	IO_L14P_15		IO_L14p_15	29	52			IO_L8P_15	A15 (Bank 15)
F16 (Bank 15) srcc	IO_L14N_15		IO_L14n_15	30	51			IO_L8N_15	A16 (Bank 15)
E15 (Bank 15) srcc	IO_L11P_15		IO_L11p_15	31	50			IO_L9P_15	A13 (Bank 15)
E16 (Bank 15) srcc	IO_L11N_15		IO_L11n_15	32	49			IO_L9N_15	A14 (Bank 15)
E18 (Bank 15)	IO_L21P_15		IO_L21p_15	33	48			IO_L4P_15	B11 (Bank 15)
D18 (Bank 15)	IO_L21N_15		IO_L21n_15	34	47			IO_L4N_15	A11 (Bank 15)
D12 (Bank 15)	IO_L6P_15		IO_L6p_15	35	46			IO_L14P_16	A10 (Bank 16) srcc
D13 (Bank 15)	IO_L6N_15		IO_L6n_15	36	45			IO_L14N_16	A9 (Bank 16) srcc
D14 (Bank 15)	IO_L1P_15		IO_L1p_15	37	44	XTMS	in		
C14 (Bank 15)	IO_L1N_15		IO_L1n_15	38	43	XTDI	in		
D15 (Bank 15) mrcc	IO_L12P_15		Gbl clock	39	42	XTDO	out		
C15 (Bank 15) mrcc	IO_L12N_15		Gbl clock	40	41	XTCK	in		

FX11LA-80P/8-SV(71)

East

J4

UART

D18 Tx	IO_L21n_15	R81 0201 1 49.9 2 Tx	1
D12 Rx	IO_L6p_15	Rx	2
D13 RTS#	IO_L6n_15		3
D14 CTS#	IO_L1p_15		4
JTAG	XTMS		5
	XTDI		6
	XTDO		7
Digilent	XTCK		8
pinout	GND		9
	+3.3V_D		10
Power in	GND		11
	+5V_in Up to 450mA		12

12 HEADER

West

+5V_in
C138
0.1uF
0201

UART pulldowns

Tx J14 Tx
Rx H15 Rx
R82 10.0k 0201
R80 10.0k 0201

01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

J3B SOUTH

sh1	sh1	END1	END1
sh2	sh2	END2	END2
sh3	sh3	sh8	sh8
sh4	sh4	sh7	sh7
sh5	sh5	sh6	sh6
Post1	Post1	Post2	Post2

FX11LA-80P/8-SV(71)

Footprint FX11L80/H/GP

CONN HEADER 80POS W/POSTS SMD
FX11LA-80P/8-SV(71) -> mezzanine

CONN RECEPT 80POS W/POSTS SMD
FX11LA-80S/8-SV(71) -> motherboard

+3.3V_D GND

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Page Contents
High density Hirose connectors

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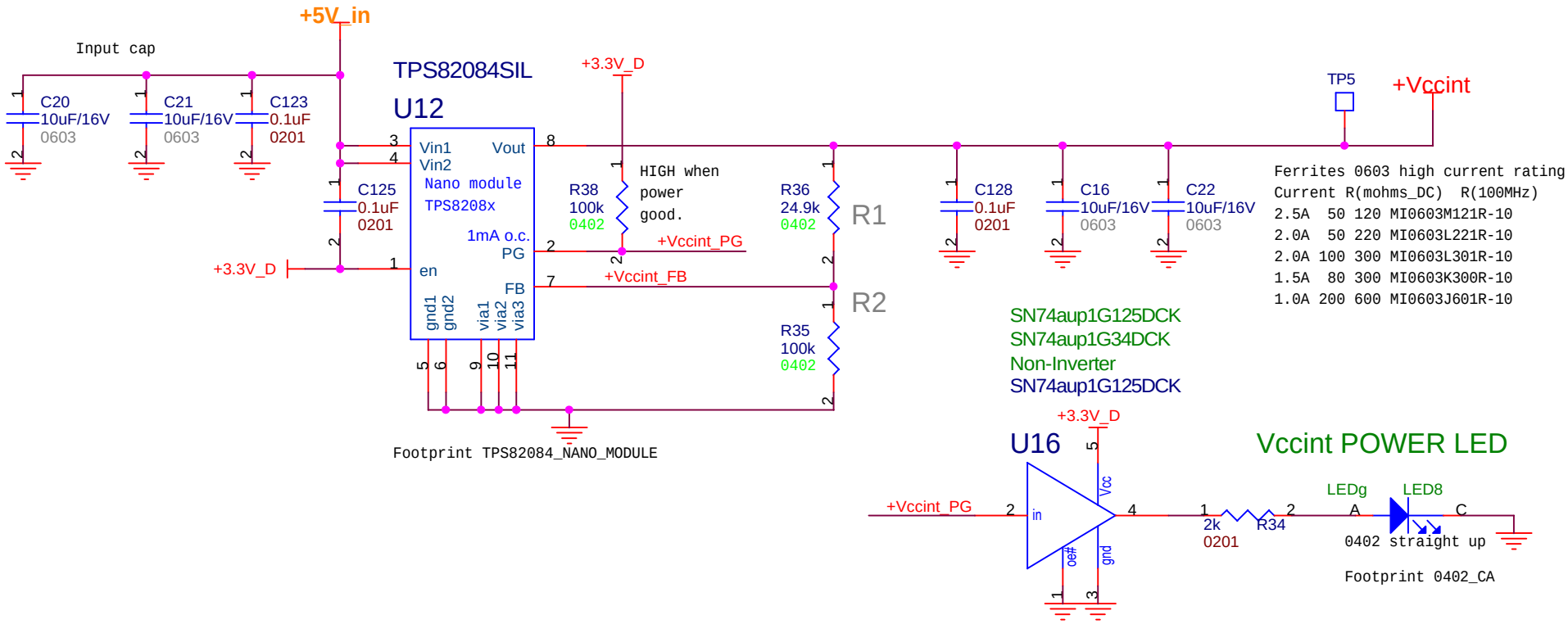
1.00V for Vccint



Ferrites 0603 high current rating

Current	R(mohms_DC)	R(100MHz)	
2.5A	50	120	MI0603M121R-10
2.0A	50	220	MI0603L221R-10
2.0A	100	300	MI0603L301R-10
1.5A	80	300	MI0603K300R-10
1.0A	200	600	MI0603J601R-10

SN74aup1G125DCK
SN74aup1G34DCK
Non-Inverter
SN74aup1G125DCK

Vccint POWER LED

SC-70 with 5 pins;
push-pull

TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
Vout = 1.00V --> R1 = 25.00k
Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
```

Need five positive voltages.
1.35V or 1.5V for DDR3L
1.8_D for FPGA & HDMI
1.0V_D for FPGA
3.3V_D for logic
Variable Vcco

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
LMZ10500SIL   $2.11  650 mA
LMZ10501SIL   $2.51  1 A
A different footprint:
TPS82084SIL   $3.11  2 A *
TPS82085SIL   $4.05  3 A *
```

01/16/2018. PRELIMINARY
prototype release for review.
Not manufactured yet.

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Page Contents
+1.35V DC/DC generator for DDR3L

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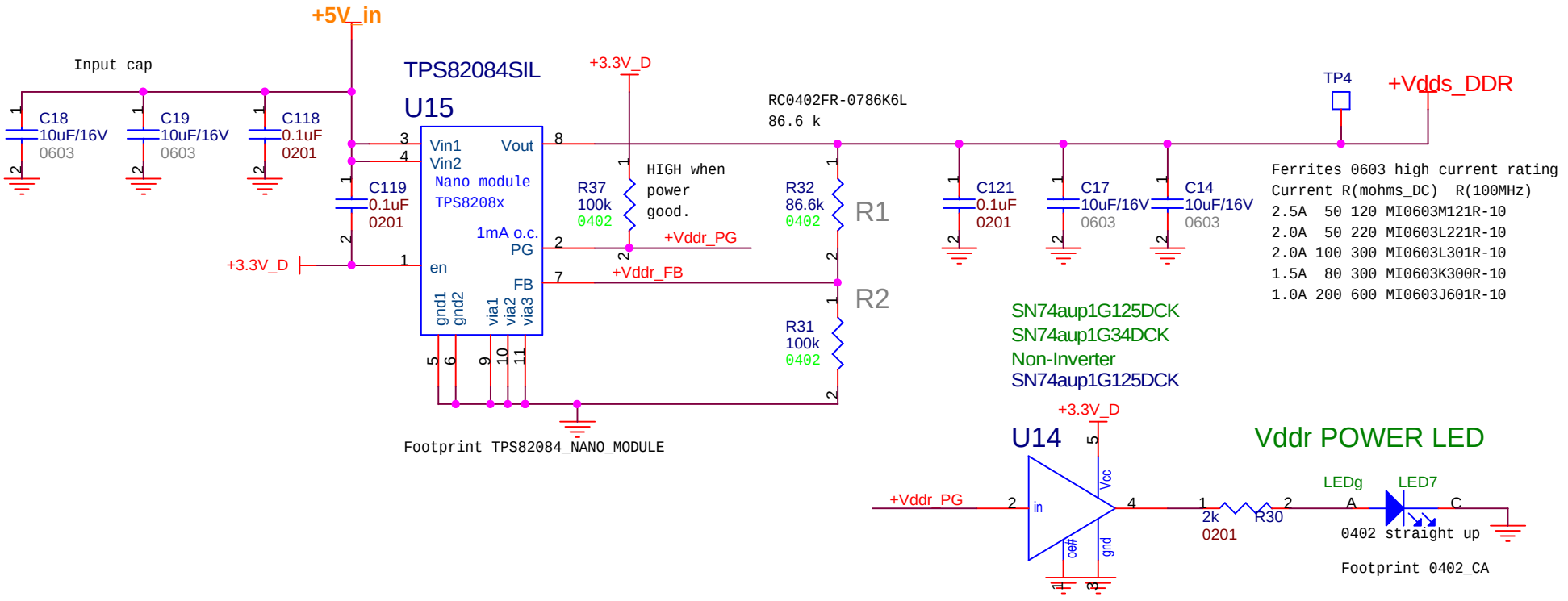
1.5V for the DDR3



TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
Vout = 1.00V --> R1 = 25.00k
Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
```

Need five positive voltages.
1.35V or 1.5V for DDR3L
1.8_D for FPGA & HDMI
1.0V_D for FPGA
3.3V_D for logic
Variable Vcco

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
LMZ10500SIL   $2.11  650 mA
LMZ10501SIL   $2.51  1 A
A different footprint:
TPS82084SIL   $3.11  2 A *
TPS82085SIL   $4.05  3 A *
```

01/16/2018. PRELIMINARY
prototype release for review.
Not manufactured yet.

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Page Contents
+1.35V DC/DC generator for DDR3L

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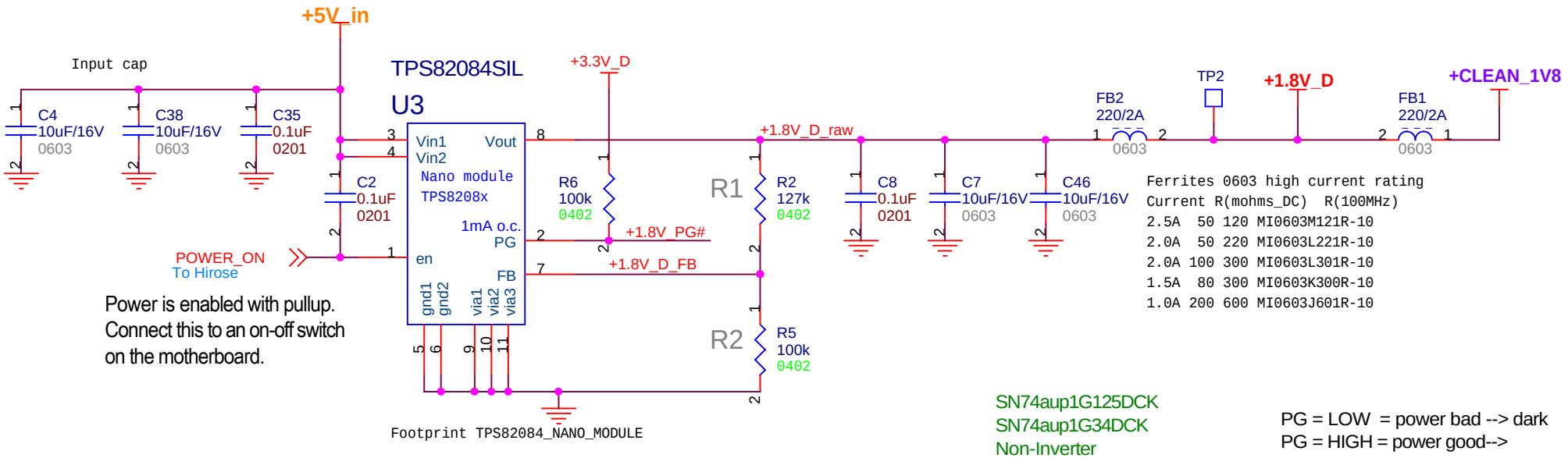
1.8V for FPGA VccAUX and for the HDMI chip

This voltage is also delivered on three North Hirose pins.

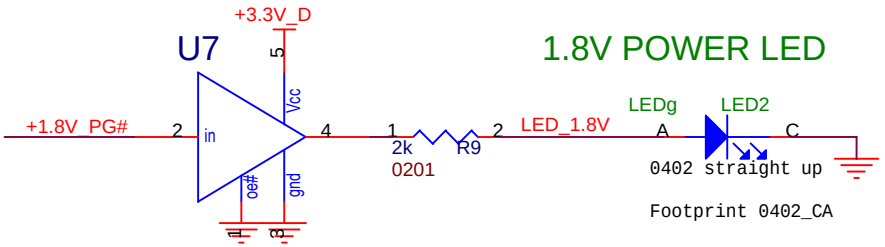


Power is enabled with pullup.
Connect this to an on-off switch
on the motherboard.

```
Ferrites 0603 high current rating
Current R(mohms_DC)  R(100MHz)
2.5A  50 120 MI0603M121R-10
2.0A  50 220 MI0603L221R-10
2.0A 100 300 MI0603L301R-10
1.5A  80 300 MI0603K300R-10
1.0A 200 600 MI0603J601R-10
```

SN74aup1G125DCK
SN74aup1G34DCK
Non-Inverter
SN74aup1G125DCK

PG = LOW = power bad --> dark
PG = HIGH = power good--> glow



1.8V POWER LED

SC-70 with 5 pins;
push-pull

TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
Vout = 1.00V --> R1 = 25.00k
Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.77V --> R1 = 121.0k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
```

Need five positive voltages.
1.35V or 1.5V for DDR3L
1.8_D for FPGA & HDMI
1.0V_D for FPGA
3.3V_D for logic
Variable Vcco

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
LMZ10500SIL   $2.11  650 mA
LMZ10501SIL   $2.51  1 A
A different footprint:
TPS82084SIL   $3.11  2 A *
TPS82085SIL   $4.05  3 A *
```

01/16/2018. PRELIMINARY
prototype release for review.
Not manufactured yet.

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Page Contents
+1.8V DC/DC generator for VccAUX, HDMI chip, and for the motherboard

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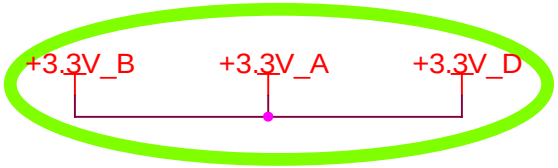
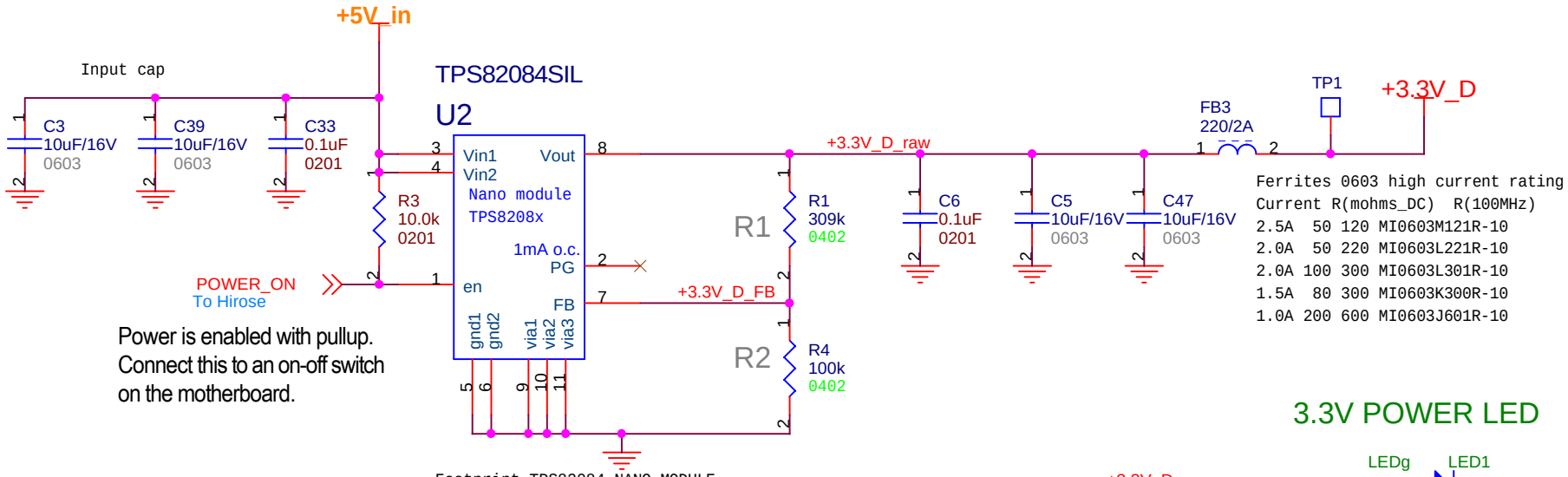
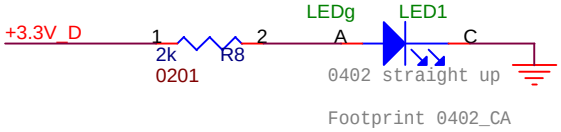
3.3V for all on-board circuits.





3.3V POWER LED



TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

```
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Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
```

Need five positive voltages.
1.35V or 1.5V for DDR3L
1.8_D for FPGA & HDMI
1.0V_D for FPGA
3.3V_D for logic
Variable Vcco

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

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A different footprint:
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TPS82085SIL   $4.05  3 A *
```

01/16/2018. PRELIMINARY
prototype release for review.
Not manufactured yet.

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Page Contents
+3.3V DC/DC generator for most of the board

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Power network names and power entry

Alter ego

+3.3V_A +3.3V_B +3.3V_D

Two banks with variable Vcco 1.2V to 3.3V

+Vcco_var

C25
10uF/16V
0603

Powered mounting holes

+3.3V_D

MTG_UL1
Upper-left

MTG_UR1
Upper-right

+Vcco_var

MTG_LL1
Lower-left

+5V_in

MTG_LR1
Lower-right

Board sketch

out
+3.3V

Hirose 80-pin

gnd

out
Vcc_variable

in
+5V

Hirose 80-pin

0.1" header JTAG

The board is powered with the lower-right mounting hole. Two other mounting holes are power outputs. One hole is ground.

TP3 TP6

01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

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Page Contents
Power network names and power entry

Size	Document Number	Rev
A	RiskFive Artix Bone	0

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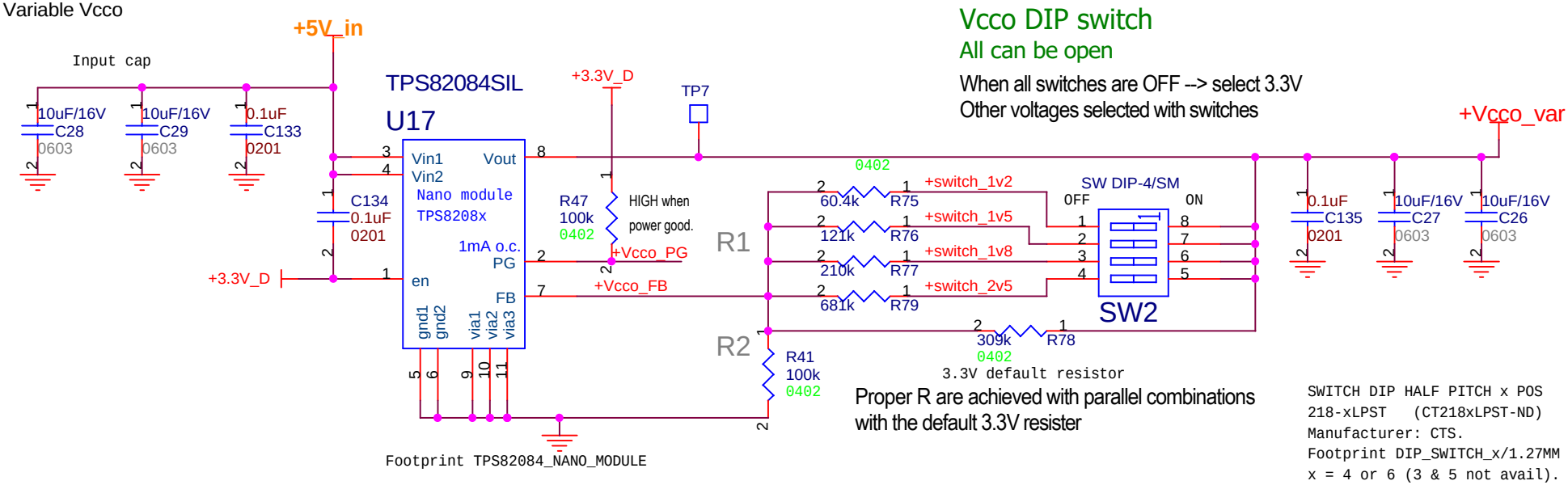
Variable Vcco for South Hirose banks 15, 16

Need five positive voltages.
1.35V or 1.5V for DDR3L
1.8_D for FPGA & HDMI
1.0V_D for FPGA
3.3V_D for logic
Variable Vcco



Vcco DIP switch

All can be open

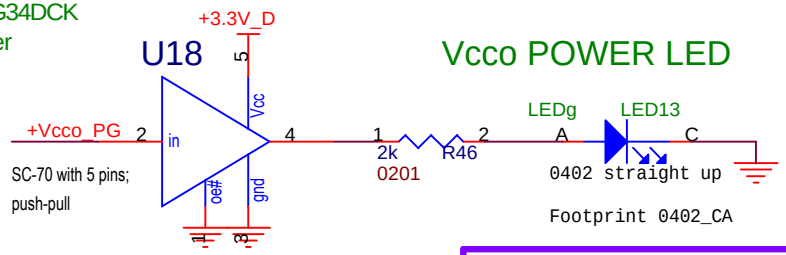
When all switches are OFF --> select 3.3V
Other voltages selected with switches

3.3V default resistor

Proper R are achieved with parallel combinations with the default 3.3V resister

```
SWITCH DIP HALF PITCH x POS
218-xLPST   (CT218xLPST-ND)
Manufacturer: CTS.
Footprint DIP_SWITCH_x/1.27MM
x = 4 or 6 (3 & 5 not avail).
```

SN74aup1G125DCK
SN74aup1G34DCK
Non-Inverter



Vcco POWER LED

```
1.20V --  60.4k RC0402FR-0760K4L
1.50V --   121k RC0402FR-07121KL
1.80V --   210k RC0402FR-07210KL
2.50V --   681k RC0402FR-07681KL
All OFF --> default 3.3V
3.30V --   309k RC0402FR-07309KL
```

```
1.2V --> 1/x = 1/50.00 - 1/309 --> x =  59.7 --> R=60.4k
1.5V --> 1/x = 1/87.50 - 1/309 --> x = 122.1 --> R=121k
1.8V --> 1/x = 1/125.0 - 1/309 --> x = 209.9 --> R=210k
2.5V --> 1/x = 1/212.5 - 1/309 --> x = 680.4 --> R=681k
```

```
Vout = 1.00V --> R1 = 25.00k
Vout = 1.20V --> R1 = 50.00k
Vout = 1.35V --> R1 = 68.75k
Vout = 1.50V --> R1 = 87.50k
Vout = 1.80V --> R1 = 125.0k
Vout = 2.50V --> R1 = 212.5k
Vout = 3.30V --> R1 = 312.5k
Assuming R2 = 100k
Use DIP switch
```

TPS82084 2A NanoModule
Vout = 0.8V*(1+R1/R2)
R1 = (1.25*Vo - 1) * R2

TPS82084T and TPS82084R are the same part.
Footprint TPS82084_NANO_MODULE

```
TPS82084SIL    $3.11   2 A *
TPS82085SIL    $4.05   3 A *
```

01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
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+1.35V DC/DC generator for DDR3L

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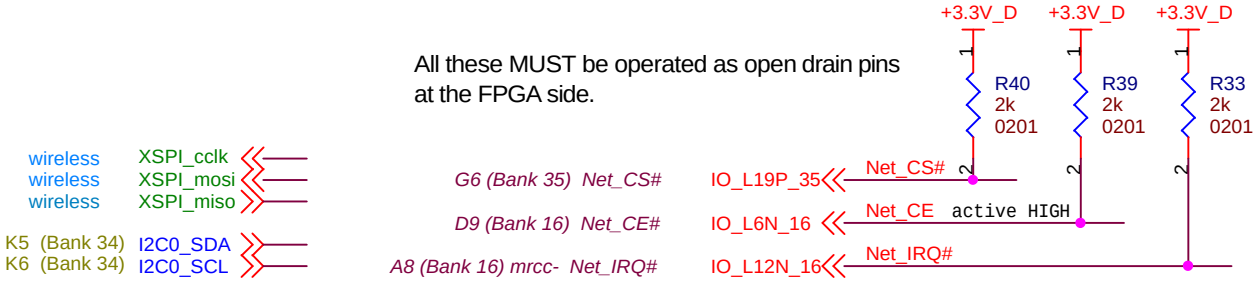
SPI & I2C connector for wireless or other uses

Possible SPI peripherals:
1) NRF24L01 module
2) Anything else.

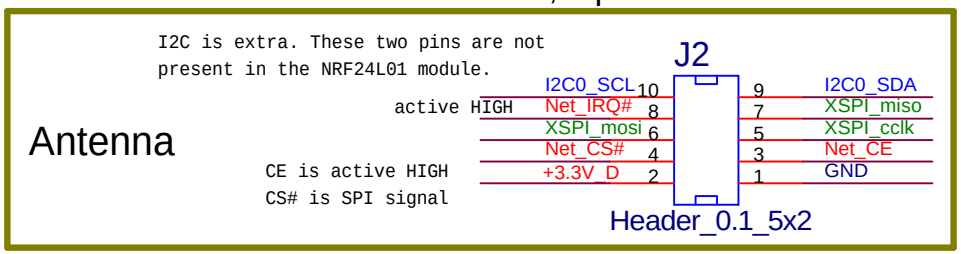
A separate connector is provided directly on the Abone, because SPI is not pinned out to Hirose. Its pinout is compatible with the NRF24L01 wireless module which was used in 2013 FPGA Oberon. Any other SPI application is possible as well.

http://www.nordicsemi.com/eng/Products/2.4GHz-RF/nRF24L01P
Nordic Semiconductor
nRF24L01P_Product_Specification_1_0.pdf; Page 50.
See also:
http://randomnerdtutorials.com/nrf24l01-2-4ghz-rf-transceiver-module-with-arduino/
https://gadgetperfect.wordpress.com/nrf24l001-rf-module2-4ghzinterfacing/

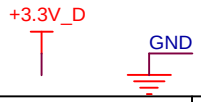
All these MUST be operated as open drain pins at the FPGA side.



NRF24L01 module, top view



01/16/2018. PRELIMINARY prototype release for review. Not manufactured yet.



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