RiskFive FPGA Module Development Motherboard

REV	Description	DATE	BY
0	01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.	01/10/2018	ws
1			
2			

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

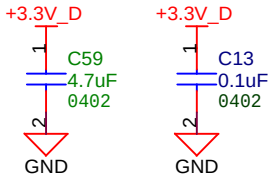
SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 103
West Henrietta, NY 14586 - 9687
http://www.skutek.com

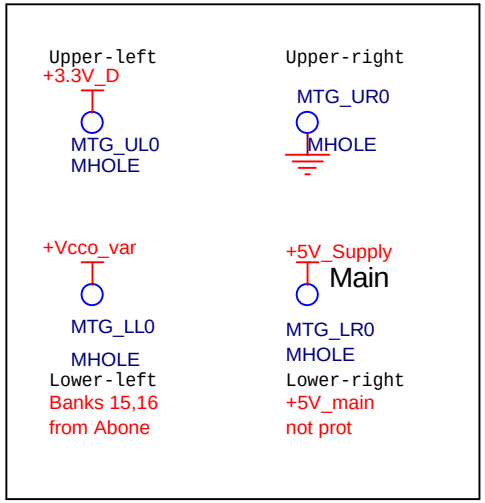
Page Contents
A - Revision page

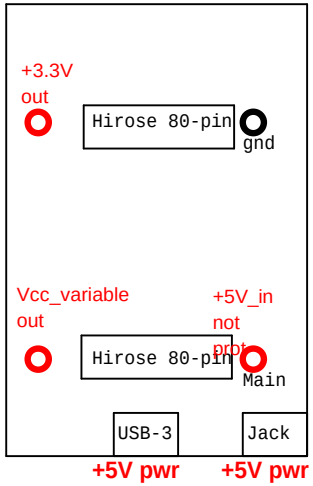
Size	Document Number	Rev
A	RiskFive Development Board	0

Date: Tuesday, January 09, 2018 Sheet 11 of 26

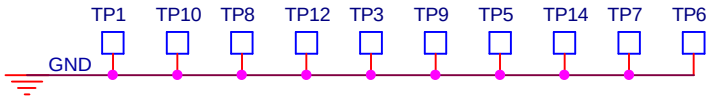
Power for the RiskFive ABone Rev 0 DUT







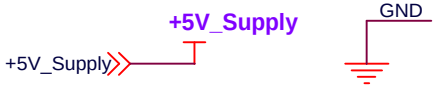
GND posts for attaching scope probes



Test point eyelets Keystone

5000	36-5000-ND	red
5001	36-5001-ND	black
5003	36-5003-ND	orange
5004	36-5004-ND	yellow
5117	36-5117-ND	blue

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.



SkuTek Instrumentation
150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents: Main power entry

Size	Document Number	Rev
A	RiskFive Development Board	0

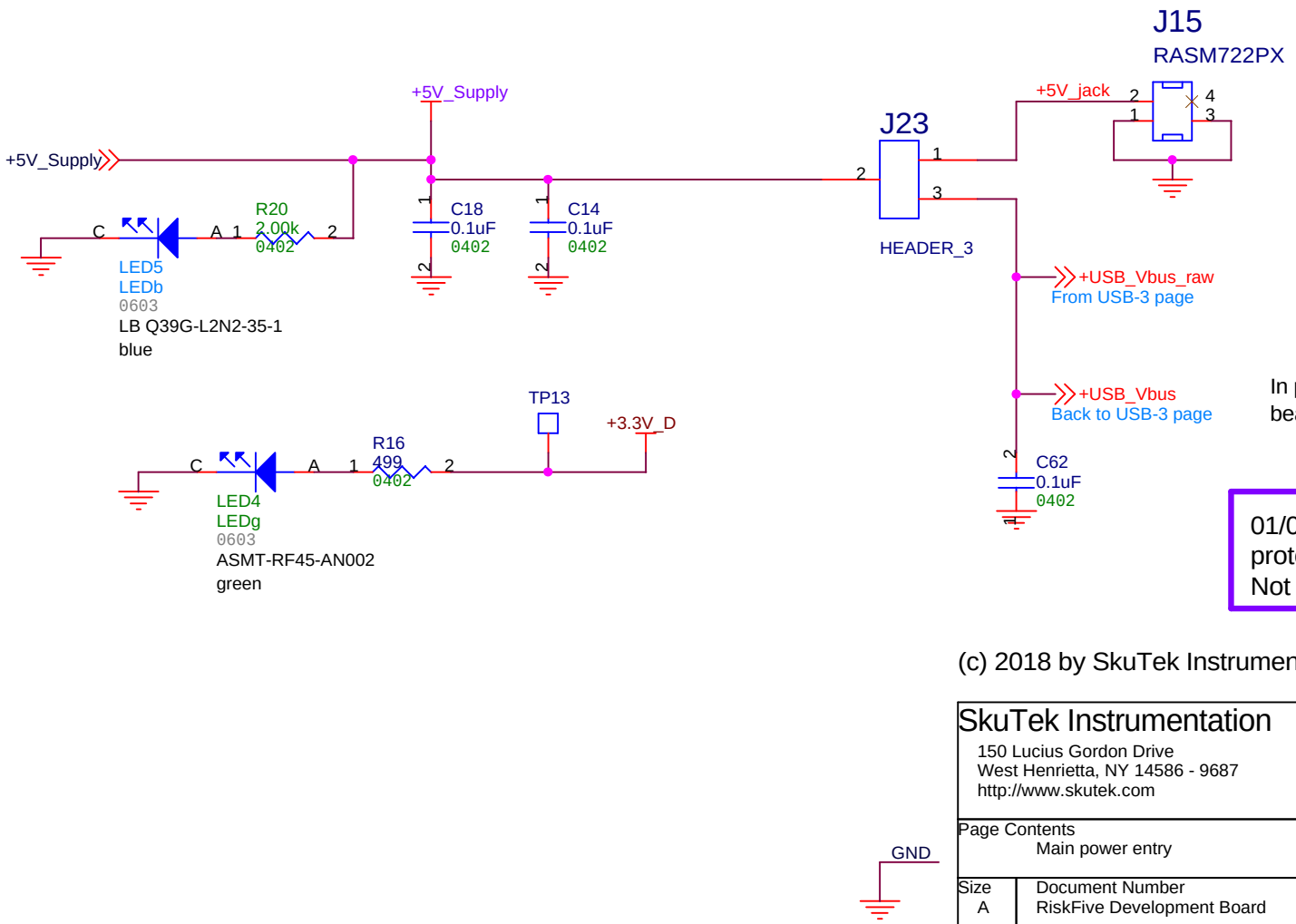
Date: Tuesday, January 09, 2018 Sheet 16 of 22

Power entry for the motherboard

RASM712PX = CONN JACK R/A .100" PIN SMD (2.5mm)
RASM722PX = CONN JACK R/A .080" PIN SMD (2.1mm)
P means locating post as an option
Contact rating: 3A

Recommended power supplies from Jameco with 2.1 mm:
379623 Mean Well GS25U05-P1J 5V/4A
1952863 Mean Well GS18U05-P1J 5A/3A

Recommended power supplies from Jameco with 2.5 mm:
2167664 FAIRWAY WN20U-050 5V/3A



In principle, I could filter Vbus with a bead, but I chose not to.

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
Main power entry

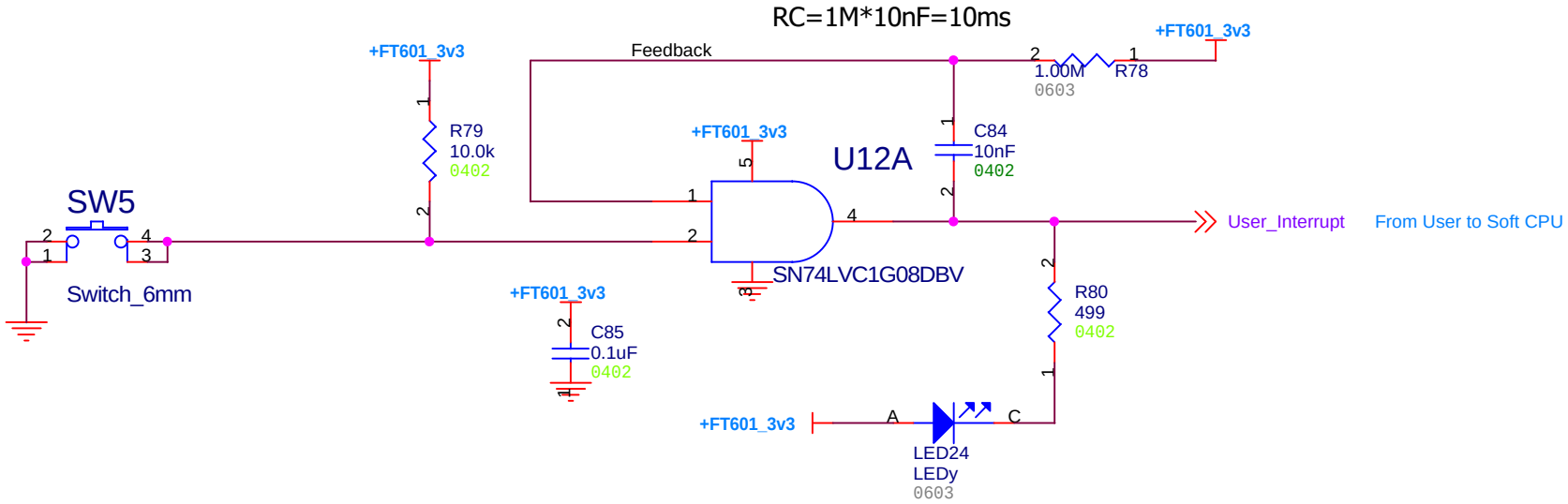
Size	Document Number	Rev
A	RiskFive Development Board	0

Date: Tuesday, January 09, 2018 Sheet 6 of 22

Push button and LED blinker

This circuit is a debouncer. FW debouncing is not needed.
Stationary output: HIGH. Push the button for LOW pulse.

This circuit is for manual interrupt generation and testing.



01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Group 4

SkuTek Instrumentation

150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
ADC test driven with the I2C0 test, and in/out for loopback tests

Size	Document Number	Rev
A	RiskFive Development Board	0

Date: Tuesday, January 09, 2018 Sheet 15 of 22

GND
GND

NORTH header

DOWN inside brd

UP outside brd

J5A

23 pins

		W5300_D5	1	1	80	80	POWER_OFF/ON		
U14 (Bank 14)	IO_L22P_14	W5300_D4	2	2	79	79	W5300_D15	POWER_ON	HIGH to Enable 3.3V_D
V14 (Bank 14)	IO_L22N_14	W5300_D3	3	3	78	78	W5300_D14	IO_L14P_14	T14 Bank_14_SRCC
T13 (Bank 14)	IO_L23P_14	W5300_D2	4	4	77	77	W5300_D13	IO_L14N_14	T15 Bank_14_SRCC
U13 (Bank 14)	IO_L23N_14	W5300_D1	5	5	76	76	W5300_D12	IO_L5P_14	R12 (Bank 14)
U12 (Bank 14)	IO_L20P_14	W5300_D0	6	6	75	75	W5300_D11	IO_L5N_14	R13 (Bank 14)
V12 (Bank 14)	IO_L20N_14	CPU_SOFT_Reset#	7	7	74	74	W5300_D10	IO_L19P_14	T11 (Bank 14)
R11 Embedded SW reset	IO_0_14	W5300_A9	8	8	73	73	W5300_D9	IO_L19N_14	U11 (Bank 14)
V10 (Bank 14)	IO_L21P_14	W5300_A8	9	9	72	72	W5300_D8	IO_L24P_14	T9 (Bank 14)
V11 (Bank 14)	IO_L21N_14	W5300_A7	10	10	71	71	W5300_D7	IO_L24N_14	T10 (Bank 14)
R10 Single ended	IO_25_14	Reserved FPGA	11	11	70	70	W5300_D6	IO_L21P_34	U9 (Bank34)
P10 FPGA conf	X_DONE	W5300_A6	12	12	69	69	Reserved FPGA	IO_L21N_34	V9 (Bank34)
R8 (Bank34)	IO_L24P_34	W5300_A5	13	13	68	68		X_PRGM#	P9 FPGA conf
T8 (Bank34)	IO_L24N_34	W5300_A4	14	14	67	67		TDA_blue7	U4 Blue7_LCD_4
U8 Single ended	IO_25_34	W5300_IRQ#	15	15	66	66		TDA_blue6	U3 Blue6_LCD_3
N16 (Bank 14)	IO_L11N_14	W5300_A3	16	16	65	65		TDA_blue5	U2 Blue5_LCD_2
U7 (Bank34)	IO_L22P_34	W5300_A2	17	17	64	64		TDA_blue4	U1 Blue4_LCD_1
U6 (Bank34)	IO_L22N_34	W5300_A1	18	18	63	63		TDA_blue3	T6 Blue3_LCD_0
V7 (Bank34)	IO_L20P_34	W5300_WR#	19	19	62	62		TDA_blue2	T3 Blue2; srcc-
V6 (Bank34)	IO_L20N_34	W5300_RD#	20	20	61	61		TDA_blue1	T1 Blue1
V5 (Bank34)	IO_L10P_34	W5300_CS#	21	21	60	60		TDA_blue0	R3 Blue0; srcc+
V4 (Bank34)	IO_L10N_34	W5300_brdy0	22	22	59	59		TDA_gr0	R6 Green0
T5 Bank_34_clk+	IO_L12P_MRCC	W5300_brdy1	23	23	58	58		TDA_gr1	R5 Green1
T4 Bank_34_clk-	IO_L12N_MRCC	W5300_brdy2	24	24	57	57		TDA_gr2	R2 Green2_LCD_5
V2 (Bank34)	IO_L9N_34	W5300_brdy3	25	25	56	56		TDA_gr3	R1 Green3_LCD_6
V1 (Bank34)	IO_L7N_34		26	26	55	55		TDA_gr4	P5 Green4_LCD_7; mrcc-
HDMI	HDMI_HPD		27	27	54	54		TDA_gr5	P4 Green5_LCD_8; srcc+
HDMI	HDMI_CEC		28	28	53	53		TDA_gr6	P3 Green6_LCD_9; srcc-
HDMI	HDMI_DSCL		29	29	52	52		TDA_gr7	P2 Green7_LCD_10
HDMI	HDMI_DSDA		30	30	51	51		TDA_red0	N2 Red0
HDMI	HDMI_TX2-		31	31	50	50		TDA_red1	N1 Red1
HDMI	HDMI_TX2+		32	32	49	49		TDA_red2	N4 Red2
+CLEAN_1V8			33	33	48	48		TDA_red3	R7 Red3_LCD_11
HDMI	HDMI_TX1-		34	34	47	47		TDA_red4	N6 Red4_LCD_12
HDMI	HDMI_TX1+		35	35	46	46		TDA_red5	M3 Red5_LCD_13
HDMI	HDMI_TX0-		36	36	45	45		TDA_red6	M2 Red6_LCD_14
HDMI	HDMI_TX0+		37	37	44	44		TDA_red7	M1 Red7_LCD_15
			38	38	43	43		TDA_PCLK	M4 TDA Video Pixel_clk
HDMI	HDMI_TXC-		39	39	42	42		TDA_DE	M6 TDA Video Data Enable
HDMI	HDMI_TXC+		40	40	41	41		TDA_SYNC_V	L1 TDA V_sync
								TDA_SYNC_H	L3 TDA H_sync

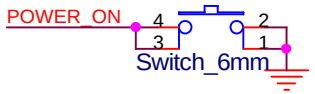
FX11LA-80S/8-SV(71)

5 pins

Total 28

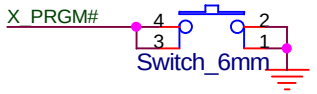
Power Cycle

SW2



FPGA Reset and Reload

SW3



To Soft CPU CPU_SOFT_Reset#

33 pins

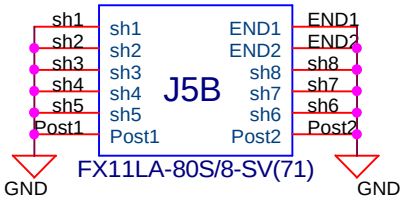
W5300_WR#
W5300_RD#
W5300_CS#
W5300_IRQ#
W5300_brdy[3:0]
W5300_A[9:1]
W5300_D[15:0]

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Footprint FX11L80/R/GP

CONN HEADER 80POS W/POSTS SMD
FX11LA-80P/8-SV(71) -> mezzanine

CONN RECEPT 80POS W/POSTS SMD
FX11LA-80S/8-SV(71) ->
motherboard



GND

SkuTek Instrumentation
150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
MBone connectors

Size	Document Number	Rev
A	RiskFive Development Board	0

Date: Tuesday, January 09, 2018 Sheet 7 of 22

SOUTH header

DOWN outside brd

UP inside brd

UART — All these are reserved on Abone

D18 Tx	IO_L21n_15	UART_chip_Tx	To RS-232 UART_chip_Tx
D12 Rx	IO_L6p_15	UART_chip_Rx	
D13 RTS#	IO_L6n_15	Optional	To RS-232 UART_chip_Rx
D14 CTS#	IO_L1p_15	Optional	
C14 extra	IO_L1n_15	Optional	

J10A

GbE	Ether_LED0	GbE	1	80	GbE	Ether_LED1	LED or PTP
GbE	Ether2+	GbE	2	79	GbE	Ether0+	GbE
GbE	Ether2-	GbE	3	78	GbE	Ether0-	GbE
GbE	Ether3+	GbE	4	77	GbE	Ether1+	GbE
GbE	Ether3-	GbE	5	76	GbE	Ether1-	GbE
PTP Start_Frame	Ether_GPIO_0	GbE	6	75	SD_card_prot	IO_L8P_14	N14 (Bank 14)
R16 (Bank 14)	IO_L15P_14	SD_DATA1	7	74	W5500_CS#	IO_L8N_14	P14 (Bank 14)
R15 (Bank 14)	IO_L13N_14	SD_DATA2	8	73	W5500_SPI_CLK	IO_L3P_14_PUDC	L15 PUDC
L18 (Bank 14)	IO_L4P_14	SD_DATA3_CS#	9	72	W5500_MISO	IO_L24P_15	K15 (Bank 15)
M13 (Bank 14)	IO_L6N_14	SD_CMD_din	10	71	W5500_MOSI	IO_L24N_15	J15 (Bank 15)
N17 (Bank 14)	IO_L9P_14	SD_CLK	11	70	W5500_IRQ#	IO_L18N_15	G17 (Bank 15)
D10 (Bank 16)	IO_L19N_16	SD_DATA0	12	69	HW_RESET#	IO_L18P_15	H17 (Bank 15)
K16 (Bank 15, SE)	IO_25_15	FT601_D13	13	68	FT601_D0	IO_L16N_15	D17 (Bank 15)
J14 (Bank 15)	IO_L19P_15	FT601_D14	14	67	FT601_D1	IO_L16P_15	E17 (Bank 15)
H15 (Bank 15)	IO_L19N_15	FT601_D15	15	66	FT601_D2	IO_L20P_15	C16 (Bank 15)
J17 (Bank 15)	IO_L23P_15	FT601_D16	16	65	FT601_D3	IO_L20N_15	C17 (Bank 15)
J18 (Bank 15)	IO_L23N_15	FT601_D17	17	64	FT601_D4	IO_L3P_15	C12 (Bank 15)
K13 (Bank 15)	IO_L17P_15	FT601_D18	18	63	FT601_D5	IO_L3N_15	B12 (Bank 15)
J13 (Bank 15)	IO_L17N_15	FT601_D19	19	62	FT601_D6	IO_L7P_15	B16 (Bank 15)
H14 (Bank 15)	IO_L15P_15	FT601_D20	20	61	FT601_D7	IO_L7N_15	B17 (Bank 15)
G14 (Bank 15)	IO_L15N_15	FT601_D21	21	60	FT601_D8	IO_L10P_15	B18 (Bank 15)
H15 (Bank 15) mrcc	IO_L13P_15	FT601_D22	22	59	FT601_D9	IO_L10N_15	A18 (Bank 15)
G16 (Bank 15) mrcc	IO_L13N_15	FT601_D23	23	58	FT601_D10	IO_L2P_15	B13 (Bank 15)
G13 (Bank 15, SE)	IO_0_15	FT601_D24	24	57	FT601_D11	IO_L2N_15	B14 (Bank 15)
G18 (Bank 15)	IO_L22P_15	FT601_D25	25	56	FT601_D12	IO_L11P_16	C9 (Bank 16) srcc
F18 (Bank 15)	IO_L22N_15	FT601_D26	26	55	FT601_OE#	IO_L11N_16	B9 (Bank 16) srcc
F13 (Bank 15)	IO_L5P_15	FT601_D27	27	54	FT601_CLK_out	IO_L13P_16	C11 (Bank 16) mrcc
F14 (Bank 15)	IO_L5N_15	FT601_D28	28	53	FT601_Wakeup#	IO_L13N_16	C10 (Bank 16) mrcc
F15 (Bank 15) srcc	IO_L14P_15	FT601_D29	29	52	FT601_GPIO0	IO_L8P_15	A15 (Bank 15)
F16 (Bank 15) srcc	IO_L14N_15	FT601_D30	30	51	FT601_GPIO1	IO_L8N_15	A16 (Bank 15)
E15 (Bank 15) srcc	IO_L11P_15	FT601_D31	31	50	PS2_clk1 PS/2	IO_L9P_15	A13 (Bank 15)
E16 (Bank 15) srcc	IO_L11N_15	FT601_BE1	32	49	PS2_d1 PS/2	IO_L9N_15	A14 (Bank 15)
E18 (Bank 15)	IO_L21P_15	FT601_BE0	33	48	PS2_d2 PS/2	IO_L4P_15	B11 (Bank 15)
UART Tx D18 (Bank 15)	IO_L21N_15	D18 Tx	34	47	PS2_clk2 PS/2	IO_L4N_15	A11 (Bank 15)
UART Rx D12 (Bank 15)	IO_L6P_15	D12 Rx	35	46	User_Interrupt	IO_L14P_16	A10 (Bank 16) srcc
Option: UART rts# D13 (Bank 15)	IO_L6N_15	FT601_BE2	36	45	User_LED	IO_L14N_16	A9 (Bank 16) srcc
Option: UART cts# D14 (Bank 15)	IO_L1P_15	FT601_BE3	37	44	XTMS in		
Option: UART xtra C14 (Bank 15)	IO_L1N_15	FT601_Tx_empty#	38	43	XTDI in		
D15 (Bank 15) mrcc	IO_L12P_15	FT601_Rx_full#	39	42	XTDO out		
C15 (Bank 15) mrcc	IO_L12N_15	FT601_WR#	40	41	XTCK in		

26

45

FX11LA-80S/8-SV(71)

SD_card_prot — Full size

SD_DATA1, SD_DATA0, SD_CLK, SD_CMD_din, SD_DATA3_CS#, SD_DATA2 — Both micro and full

W5300 is on North Hirose

	W5500_IRQ#
SPI	W5500_MISO
SPI	W5500_MOSI
SPI	W5500_SPI_CLK
Chip sel	W5500_CS#

User interrupt testing

From Soft CPU	HW_RESET#
To Soft CPU	User_Interrupt

PS/2: PS2_clk1, PS2_d1, PS2_d2, PS2_clk2

USB-3

FT601_D[31:0]
FT601_BE[3:0]
FT601_Tx_empty#
FT601_Rx_full#
FT601_WR#
FT601_RD#
FT601_OE#
FT601_WAKEUP#
FT601_GPIO0
FT601_GPIO1
FT601_CLK_out

R82 499 — R81 499 0402 — LED25 LEDy 0603 — User interrupt testing

JP1 — Scope test point — HEADER 2

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

J10B

sh1	sh1	END1	END1
sh2	sh2	END2	END2
sh3	sh3	sh8	sh8
sh4	sh4	sh7	sh7
sh5	sh5	sh6	sh6
Post1	Post1	Post2	Post2

FX11LA-80S/8-SV(71)

GND GND GND GND

Footprint FX11L80/R/GP

CONN HEADER 80POS W/POSTS SMD
FX11LA-80P/8-SV(71) -> mezzanine

CONN RECEPT 80POS W/POSTS SMD
FX11LA-80S/8-SV(71) ->
motherboard

SkuTek Instrumentation
150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

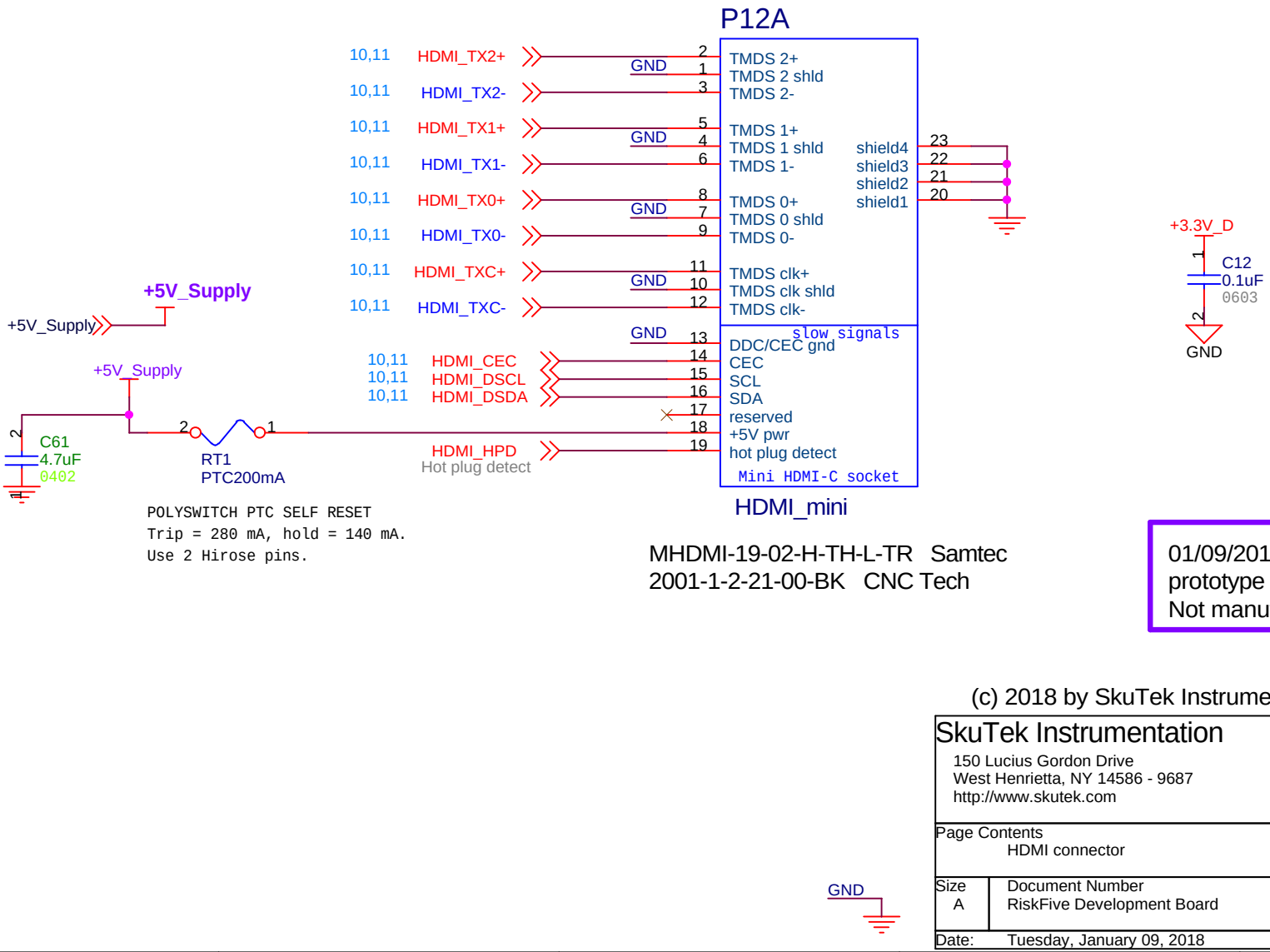
Page Contents: MBone connectors

Size	Document Number	Rev
A	RiskFive Development Board	0

Date: Tuesday, January 09, 2018 — Sheet 17 of 22

HDMI-C Mini Receptacle

Pin layout for the HDMI cable without Ethernet



MHDMI-19-02-H-TH-L-TR Samtec
2001-1-2-21-00-BK CNC Tech

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

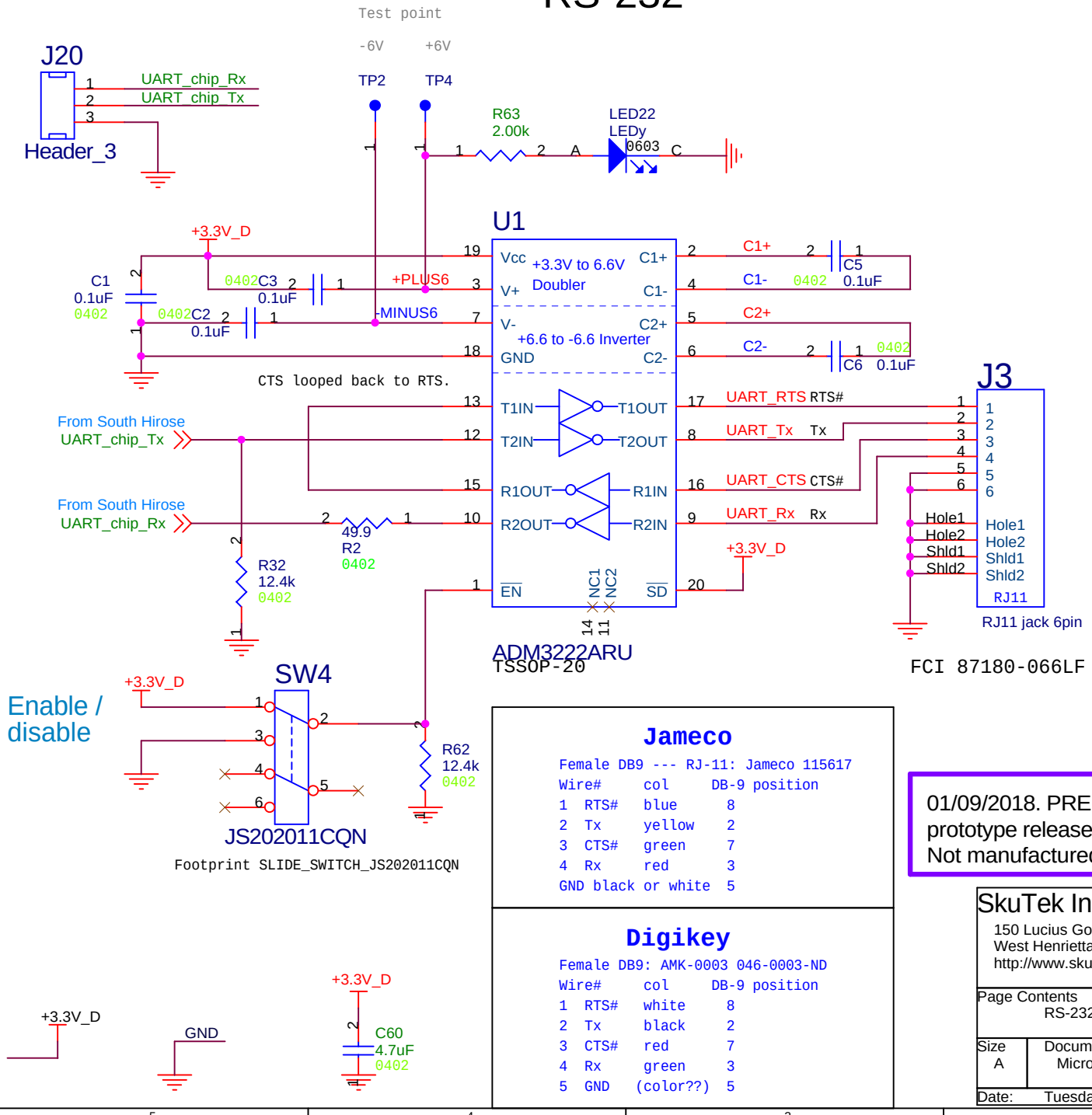
Page Contents
HDMI connector

Size	Document Number	Rev
A	RiskFive Development Board	0

Date: Tuesday, January 09, 2018 Sheet 8 of 22

Pin header for the FTDI USB-UART cable. While using the FTDI the RS232 must be disabled.

RS-232



Jameco

Female DB9 --- RJ-11: Jameco 115617

Wire#	col	DB-9 position
1 RTS#	blue	8
2 Tx	yellow	2
3 CTS#	green	7
4 Rx	red	3
GND	black or white	5

Digikey

Female DB9: AMK-0003 046-0003-ND

Wire#	col	DB-9 position
1 RTS#	white	8
2 Tx	black	2
3 CTS#	red	7
4 Rx	green	3
5 GND	(color??)	5

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

DB9 pin description

pin	PC(DTE) Function	BF Function
3	Transmit Data	Rx
2	Receive Data	Tx
7	Request to Send	RTS#
8	Clear to Send	CTS#

Software flow control is expected because CTS and RTS are looped back.

On-board RS-232 modular jack

A DB9 connector is too large for the board. Telephone-style jack with 6 pins is used instead. RS-232 pins are not assigned for such jacks. A configurable adapter is used to reassign the pins after the board is deployed.

TYCO RJ11-6Nxxxx $5 (about)
FCI 87180-066LF 609-1057-ND $1.41

Configurable adapter RJ11 --> DB9 by CUI
Male DB9: AMK-0002 046-0002-ND $4.13
Female DB9: AMK-0003 046-0003-ND $4.13

Jameco part numbers (six wire):
66203 Mfg: 31D1-16400-R $2.79

RJ cable

6-wire RJ cable between the adapter and the jack from I.O. Interconnect:

2.1m GLF-466-076-510-D H1663R-07-ND $3.34
7.6m GLF-466-256-511-D H1662R-25-ND $5.54

Jameco part number (7 feet, six wires 6P6C):
115617 Mfg: 306-707SL $1.99

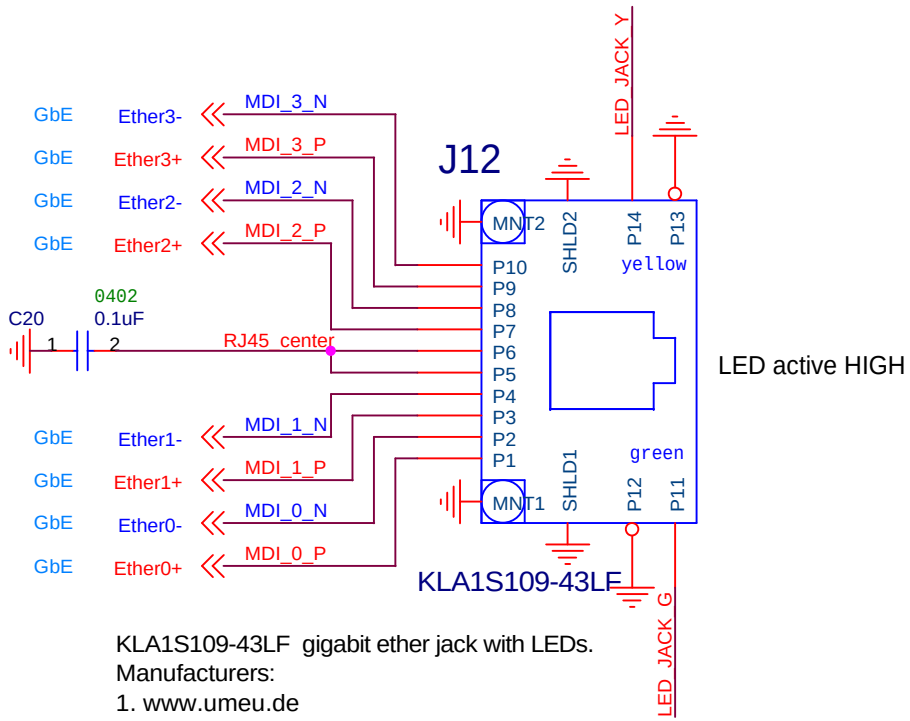
SkuTek Instrumentation
150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents: RS-232

Size	Document Number	Rev
A	MicroBone Test Board	0

Date: Tuesday, January 09, 2018 Sheet 9 of 22

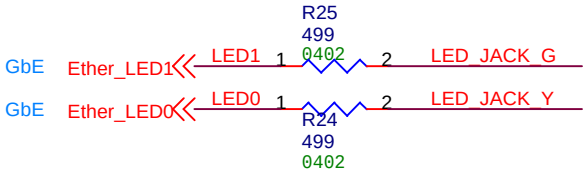
GbE jack



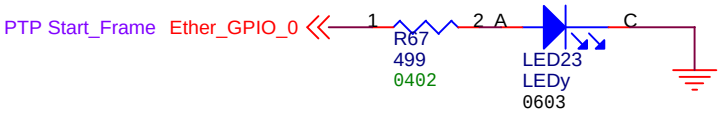
LED active HIGH

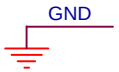
KLA1S109-43LF gigabit ether jack with LEDs.
Manufacturers:
1. www.umeu.de
2. www.bothhandusa.com

Center tap to AVdd not required. Internal on-chip termination provided on Media Dependent Interface (i.e., magnetics).



LED active HIGH





01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
GbE jack

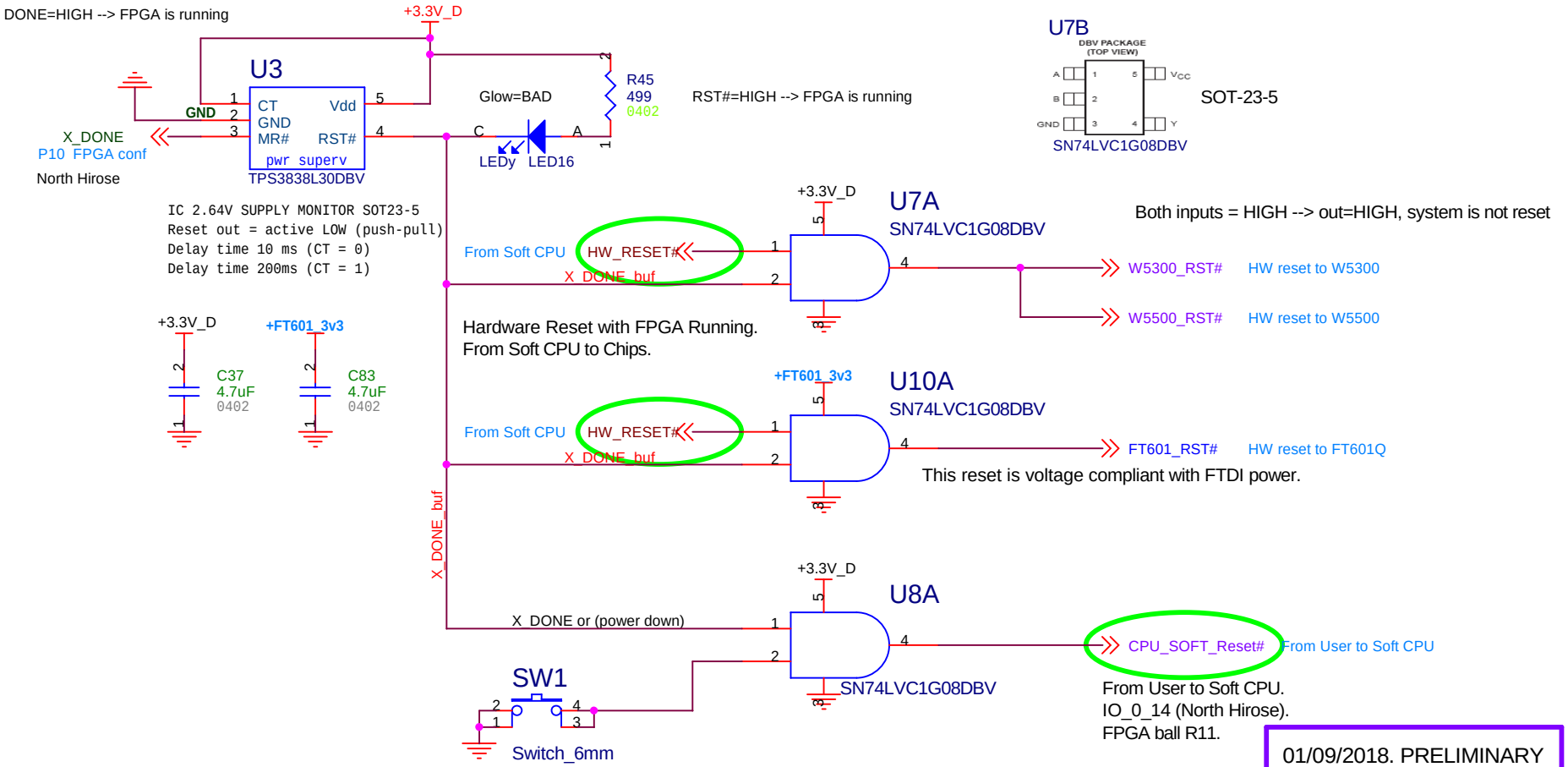
Size	Document Number	Rev
A	RiskFive Development Board	0

Date: Tuesday, January 09, 2018 Sheet 10 of 22

Reset generators

Due to shortage of connector pins we have only three reset circuits. Reset #2 does not return back to the FPGA.

1. Soft CPU reset: User Button --> FPGA Soft Core. Restart SW w/o hard FPGA reset.
2. Hardware reset Soft CPU --> all chips on this board. To be issued by the Soft CPU software.
3. FPGA Reprogram: Reload the FPGA bit file. To be issued by the operator pressing the button.
   Reset #3 is on the FPGA Configuration page.



01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Group 13

Wiznet W5300 needs a "manual reset" after being powered up. This is done automatically with X_DONE. Additionally, Soft CPU software can also issue a reset to hardware chips.

GND

GND

SkuTek Instrumentation

150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
South LED display

Size	Document Number	Rev
Custom	RiskFive Development Board	0

Date: Tuesday, January 09, 2018 Sheet 12 of 22

USB3 chip FT601Q

Footprint QFN-76_FT601Q_12_vias

+Vcco_var +FT601_3v3 FT601 is connected to Banks 15,16

U9A

FT601Q USB3 1/5

FT601_D31 76 D31
FT601_D30 75 D30
FT601_D29 74 D29
FT601_D28 73 D28
FT601_D27 72 D27
FT601_D26 71 D26
FT601_D25 70 D25
FT601_D24 69 D24
FT601_D23 67 D23
FT601_D22 66 D22
FT601_D21 65 D21
FT601_D20 64 D20
FT601_D19 63 D19
FT601_D18 62 D18
FT601_D17 61 D17
FT601_D16 60 D16
FT601_D15 57 D15
FT601_D14 56 D14
FT601_D13 55 D13
FT601_D12 54 D12
FT601_D11 53 D11
FT601_D10 52 D10
FT601_D9 51 D9
FT601_D8 50 D8
FT601_D7 47 D7
FT601_D6 46 D6
FT601_D5 45 D5
FT601_D4 44 D4
FT601_D3 43 D3
FT601_D2 42 D2
FT601_D1 41 D1
FT601_D0 40 D0

FT601_BE0 4 BE_0
FT601_BE1 5 BE_1
FT601_BE2 6 BE_2
FT601_BE3 7 BE_3

FT601Q-B-T

FT601_D[31:0]
FT601_BE[3:0]

U9B

FT601Q USB3 2/5

FT601_RST# 15 RESET#_in
FT601_WAKEUP# 16 Wakeup#
FT601_Tx_empty# 8 Tx_FIFO_Empty#
FT601_Rx_full# 9 Rx_FIFO_Full#
FT601_WR# 11 WR#_in
FT601_RD# 12 RD#_in
FT601_OE# 13 OE#_in
FT601_GPIO0 17 GPIO0
FT601_GPIO1 18 GPIO1
FT601_CLK_out R73 49.9 0402 58 CLK_out

FT601Q-B-T

FT601_OE# R70 2.00k 0402 +FT601_3v3
FT601_WR# R71 2.00k 0402 +FT601_3v3
FT601_RST# R72 2.00k 0402 +FT601_3v3

U9E

FT601Q USB3 3/5

+FT601_1v0 C63 4.7uF 1.0V TP18

LDO_1v0_out 39
Vd_1v0_in 3
Vd_1v0_in 30
Vd_1v0_in 33
Vd_1v0_in 48
AVdd_1v0_in 2
gnd4 36
gnd3 29
gnd2 26
gnd1 1

VddA_3v3_in 28
Vcc33_in 38
Vcc33_in 20
Vcc33_in 24
VccIO_in 68
VccIO_in 59
VccIO_in 49
VccIO_in 14
88 87 86 85

77 78 79 80 81 82 83 84

FT601Q-B-T

+FT601_3v3 C64 4.7uF

U9C

FT601Q USB3 3/5

SIWU#_pullup 10 R68 2.00k 0402 +FT601_3v3
reserved (nc) 19
Xtal_in 21 18pF 0402 C65
Y1 ABM7-30.000MHZ-D2Y-T
Xtal_out 22 18pF 0402 C66
Rref_1.6k 27 1.60k R69

FT601Q-B-T

U9D

FT601Q USB3 4/5

Vbus_in 37 From PWR entry page +USB_Vbus To PWR entry page +USB_Vbus_raw
USB2_Dn 25 USB2_D-
USB2_Dp 23 USB2_D+
USB3_in- 34 USB3_Rx-
USB3_in+ 35 USB3_Rx+
USB3_out- 31 USB3_out- 0.1uF C67 USB3_Tx-
USB3_out+ 32 USB3_out+ 0.1uF C68 USB3_Tx+

FT601Q-B-T

Tx needs caps

J24

USB-3.0 connector

Shield1 11
Vbus 1
USB2_D- 2
USB2_D+ 3
gnd 4 GND
USB3_Rx- 5
USB3_Rx+ 6
USB3_gnd 7 GND
USB3_Tx- 8
USB3_Tx+ 9
Shield2 10

USB 3.0 Connector

E8199-001-01

+FT601_3v3 0402 C69 C70 C71 C72 C73 C74 C75 C76 0.1uF

+FT601_1v0 0402 C77 C78 C79 C80 0.1uF

GND GND

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Crystals

ABM8G-30.000MHZ-18-D2Y-T
CRYSTAL 30.0000MHZ 18PF SMD four leads

ABM7-30.000MHZ-D2Y-T
535-9849-1-ND two leads; 1812

Group 1

SkuTek Instrumentation

150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents: USB3

Size	Document Number	Rev
Custom	MicroBone Test Board	0

Date: Tuesday, January 09, 2018 Sheet 13 of 22

SPI to Ethernet driver: Wiznet W5500

http://wizwiki.net/wiki/doku.php?id=products:w5500:start

J1B1211CCD jack is available from
http://www.shopwiznet.com/j1b1211ccd
Mouser: 950-J1B1211CCD

W5500 is available from:
http://www.shopwiznet.com/w5500
Mouser: 950-W5500
Digikey: yes, but more expensive!

W5500_LED_S C A 0603 LEDy LED12 +3.3V_D
W5500_LED_D C A LEDy LED13
W5500_LED_A C A LEDy LED14
W5500_LED_L C A LEDy LED15 0603

YELLOW

FB_0603_1A FB1 +W5500_AVdd +3.3V_D

U2

AVdd 3v3 4 15 17 21 8 11
3v3 Vdd 28
Txp 2 W5500_Tx+
Txn 1 W5500_Tx-
Rxp 6 W5500_Rx+
Rxn 5 W5500_Rx-
gnd rsvd5 42 rsvd4 41 rsvd3 40 rsvd2 39 rsvd1 38 rsvd0 23
GND AGND 29 19 16 14 9 3 48
SpdLED 24 W5500_LED_Spd
LnkLED 25 W5500_LED_Lnk
DupLED 26 W5500_LED_Dup
ActLED 27 W5500_LED_Act
Xin/CLKin 30 CLK_W5500_3v3
25MHz Xout 31
1v2out 22 C29 10nF 0402
nc1 47 nc2 46 nc3 13 nc4 7 nc5 12 nc(Vref) 18

W5500

Wiznet footprint QUAD.50M/48/WG9.00

1 1 1 All capable,
Auto-negotiation enabled

pmode0 45 pmode1 44 pmode2 43

X_DONE or (pwr down)

rst# 37 W5500_RST#
INT# 36 W5500_IRQ#

SPI MISO 34 W5500_MISO
SPI MOSI 35 W5500_MOSI
SPI SCK 33 W5500_SPI_CLK
00: Wiznet. CS# 32 W5500_CS#

ExRes 10 12.4k R39 12.4k 0402
TOCAP 20 4.7uF C28 4.7uF 0402

R34 49.9 0402
R35 49.9 0402
R36 49.9 0402
R37 49.9 0402

C24 10nF 0402
C25 10nF 0402
C27 10nF 0402

W5500_Rx_cen

R33 10.0k 0402
W5500_Tx_cen
C22 10nF 0402
C23 10nF 0402

J21

Tx+ 1
TxCent 2
Tx- 3
Rx+ 4
RxCent 5
Rx- 6
shld3 14
shld2 13
shld1 8
nc 7
RJ45
LEDg- W5500_LED_A 9
LEDg+ 10
LEDy- W5500_LED_L 11
LEDy+ 12

J1B1211CCD

Footprint
RJ45_J1B1211CCD

RJ45 recommended for W5300:
RD1-125BAG1A

Pullups
+3.3V_D R40 2.00k 0402 W5500_IRQ#
+3.3V_D R65 2.00k 0402 W5500_CS#

W5500_LED_Spd 499 R41 W5500_LED_S
W5500_LED_Lnk 499 R42 W5500_LED_L
W5500_LED_Dup 499 R43 W5500_LED_D
W5500_LED_Act 499 R44 W5500_LED_A

+3.3V_D C30 4.7uF 0402
+3.3V_D C31 0.1uF 0402
+W5500_AVdd C32 4.7uF 0402
C33 0.1uF 0402
C34 0.1uF 0402
C35 0.1uF 0402
C36 0.1uF 0402

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Group 33

+3.3V_D GND

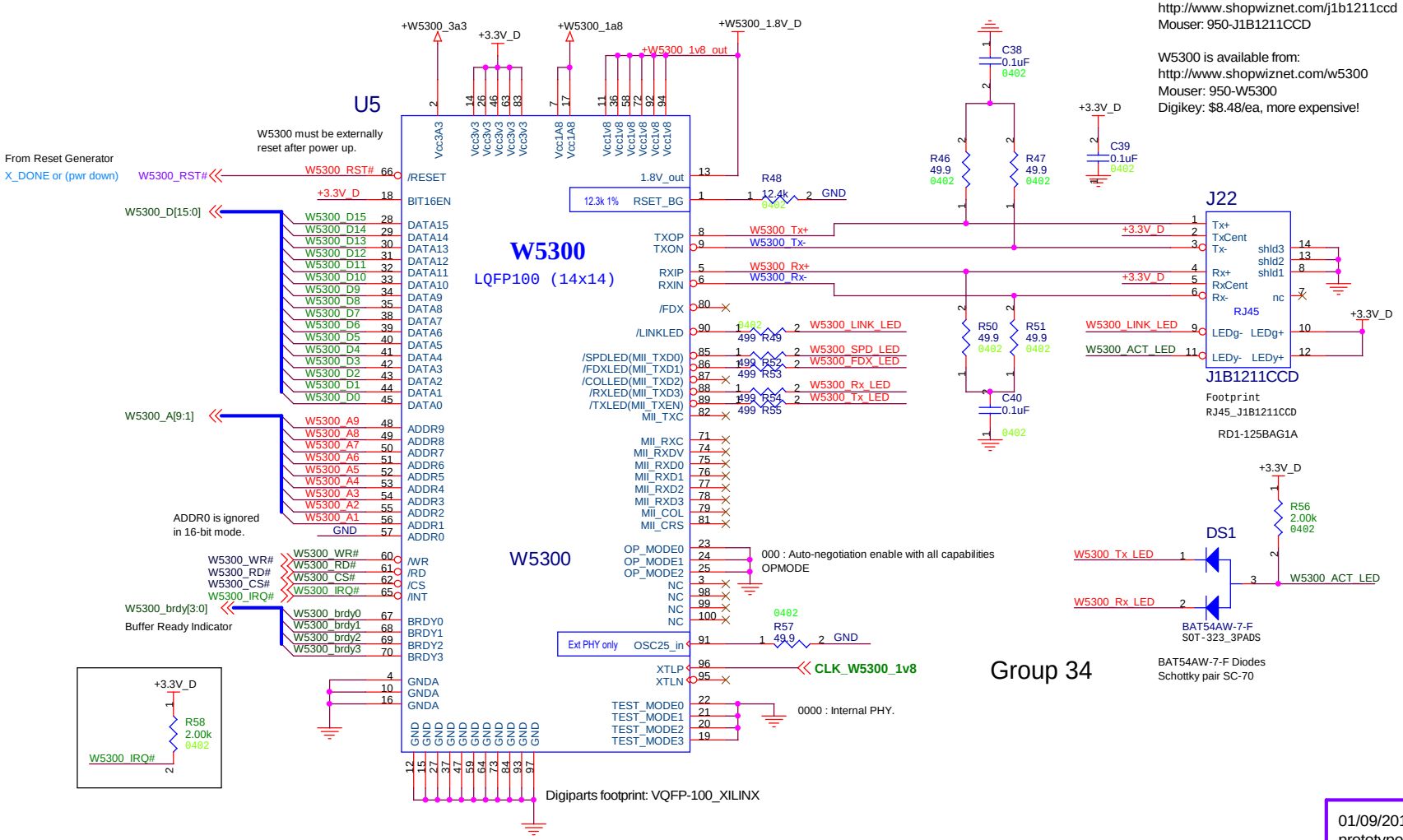
SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 103
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents: Ethernet using Wiznet

Size	Document Number	Rev
A	RiskFive Development Board	0

Date: Tuesday, January 09, 2018 Sheet 18 of 22

Ethernet controller and PHY, 16-bit interface



J1B1211CCD jack is available from
http://www.shopwiznet.com/j1b1211ccd
Mouser: 950-J1B1211CCD

W5300 is available from:
http://www.shopwiznet.com/w5300
Mouser: 950-W5300
Digikey: $8.48/ea, more expensive!

BAT54AW-7-F Diodes
Schottky pair SC-70

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

Derived from W5300 Internal PHY reference schematic

SkuTek Instrumentation
150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

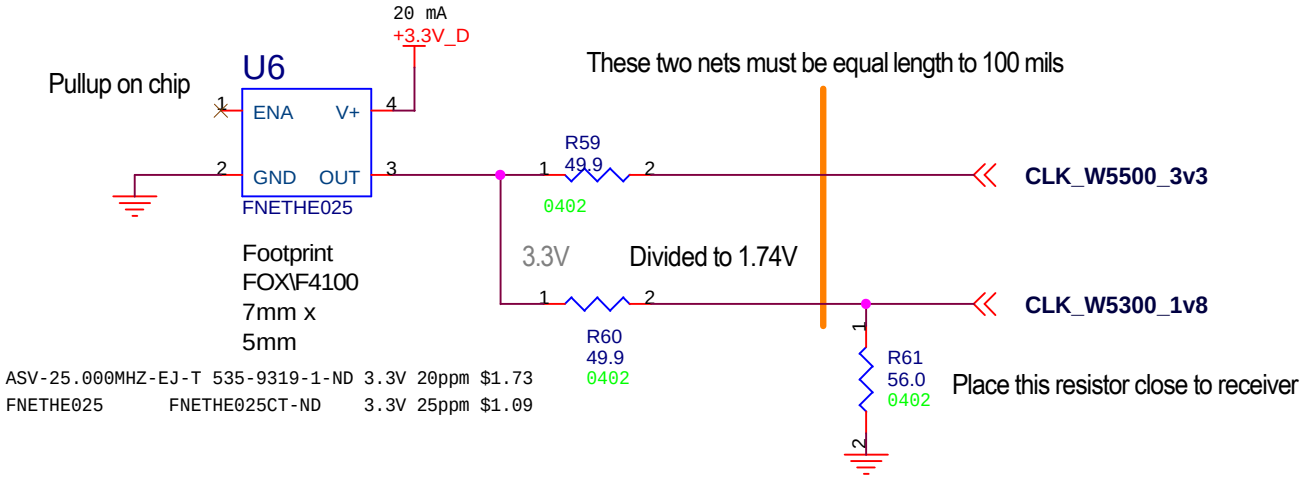
Page Contents: Ethernet using Wiznet W5300

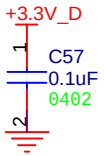
Size	Document Number	Rev
B	RiskFive Abone Development Board	0

Date: Tuesday, January 09, 2018 Sheet 19 of 22

Clock driver 100 MHz CMOS 3.3V and 1.8V

This clock is driving the Ethernet chips. In order to avoid a fan-out buffer I am using two source-terminated nets. Additionally, the W5300 clock is reduced down to 1.74V (close enough to 1.8V).





Group 12

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive, Ste. 103
West Henrietta, NY 14586 - 9687
http://www.skutek.com

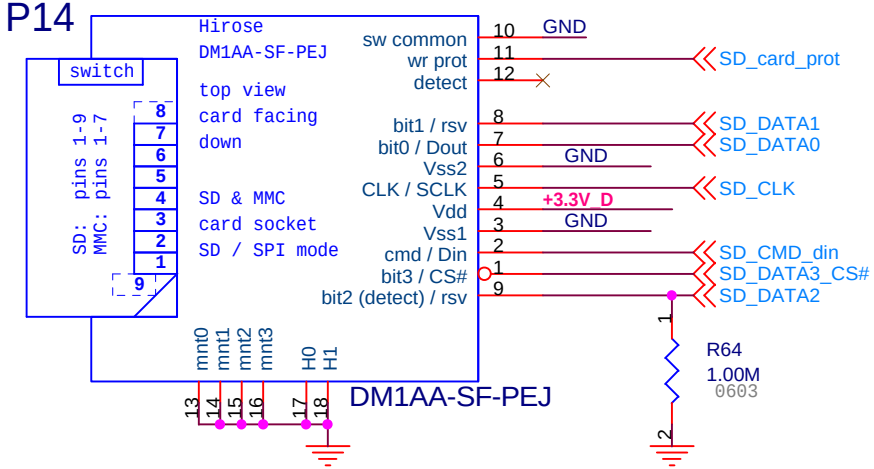
Page Contents: Ethernet clock driver

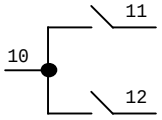
Size	Document Number	Rev
A	RiskFive Development Motherboard	0

Date: Tuesday, January 09, 2018 Sheet 20 of 22

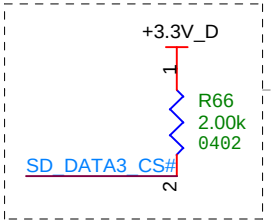
SD / MMC full size card socket

Socket SD/MMC HRS DM1AA-SF-PEJ Still available on Dec/18/2017



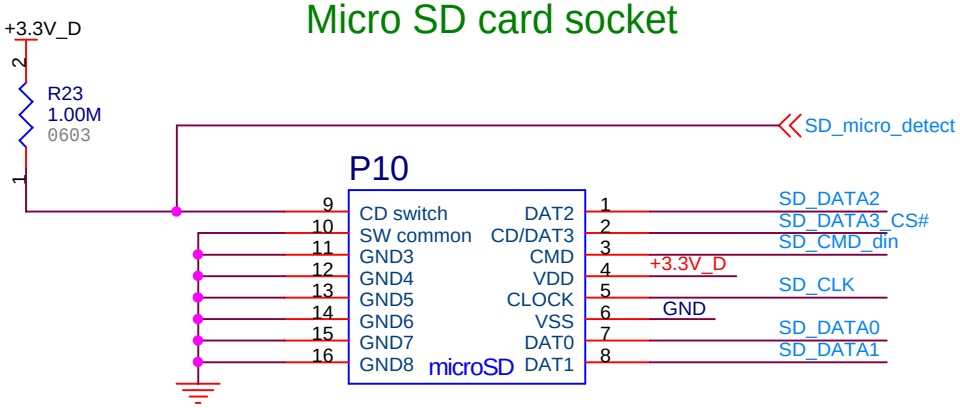


Bit2 (detect) has on-card pullup 50k used to detect the SD card. A large pulldown is needed here.



Not connected

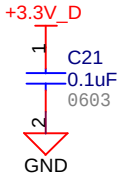
Micro SD card socket



SCHA5B0200

SD_card_prot is not connected

Mouser on Feb/05/2015
1: $1.32
25: $1.18
50: $1.10
100: $1.06



Notes

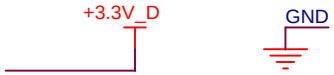
Compgroup 2 is used for initial placement.

The card detection scheme seems different from the one employed with the uSD card, while in fact they should be the same. It needs be reviewed.

The physical "protect switch" will detect the position of the "write protect" switch on the SD card. MMC card does not have that switch. Pullups are needed.

DM1AA-SF-PEJ - SD Memory Card Connectors - Hirose Electric
DigiKey HR845CT-ND $4.67

Card detect not implemented due to shortage of Hirose pins



01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.

SkuTek Instrumentation
150 Lucius Gordon Drive
West Henrietta, NY 14586 - 9687
http://www.skutek.com

Page Contents
SD card sockets

Size	Document Number	Rev
A	RiskFive Development Board	0

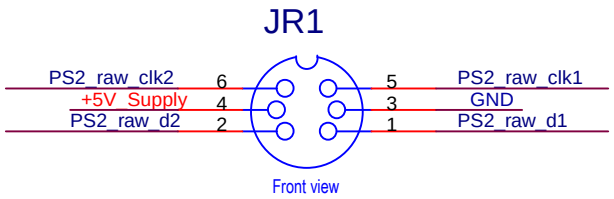
Date: Tuesday, January 09, 2018 Sheet 21 of 22

PS2 connectors

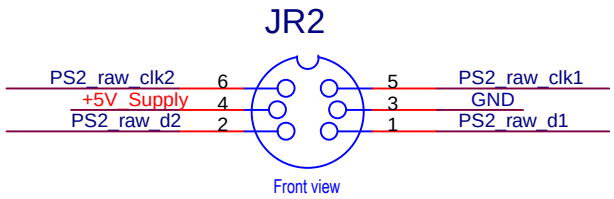
http://www.burtonsys.com/PS2_keyboard_and_mouse_mini-DIN-6_connector_pinouts.html
http://pinouts.ru/InputCables/Ps2KeyboardYThinkpad.shtml
http://pinouts.ru/Inputs/KeyboardPC6_pinout.shtml

Alternatively, this connector can be used as GPIO with 5V levels.

PS2 connector is 6-pin Mini DIN
Footprint in the DIN library
DINC/MIN_TM/6 is REVERSED
Fixed in Digiparts.LLB



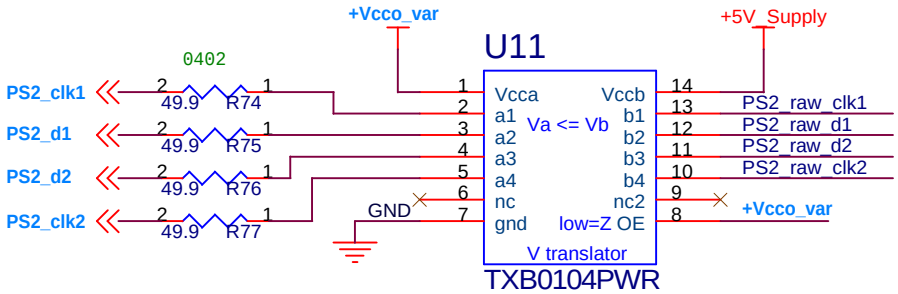
Mouse

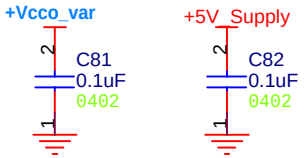


Keyboard

Use low driving current and serial termination at the FPGA side.

TXS0104 has OC outputs with 4k pullup on chip.
TXB0104 has push-pull outputs.
OE active HIGH (!) is referenced to Vcca.





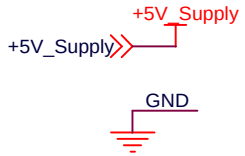

```
Mouse / keyboard Vcc = 5V
FPGA only tolerates 4V

http://pinouts.ru/InputCables/Ps2KeyboardYThinkpad.shtml
Con  signal  Keybrd     Mouse
1    dat1      ----    1 (data)
2    dat2   1 (data)    ----
3    gnd    3 (gnd)   3 (gnd)
4    Vcc    4 (Vcc)   4 (Vcc)
5    clk1      ----    5 (clk)
6    clk2   5 (clk)     ----
```

http://www.computer-engineering.org/ps2protocol/
Summary: Power Specifications
Vcc = +4.5V to +5.5V.
Max Current = 275 mA.

Voltage trans 4bit TXB0104PWR
SOG.65M/14/WG6.50/L5.0

Group 25

01/09/2018. PRELIMINARY prototype release for review. Not manufactured yet.



SkuTek Instrumentation - W. Henrietta, NY		
Title: Logic IO for PS2 or general purpose 5V logic IO		
Size	Document Number: RiskFive Development Board	Rev: 0
Date: Tuesday, January 09, 2018	Sheet 22 of 22	